4245 69579

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Date 6/24/02 Serial # 09/893,487 Priority Application Date 6/29/01

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-15

Prob See Page 1 Lines 9-27
" " 2 " 1-5
" " 3 " 23-27
" " 4 " 1-4

Solution " " 4 " 6-27
" " 5 " 1-17

Novelty inherent (See Claims)

Staff Use Only	Type of Search	Vendors
Searcher: Derrick Blalock	Structure (#)	STN ✓
Searcher Phone:	Bibliographic ✓	Dialog
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 6/24/02	Fulltext	Lexis-Nexis
Date Completed: 6/28/02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 60	Other	Other
Online Time: 140		

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     FILE 'REGISTRY' ENTERED AT 07:44:20 ON 28 JUN 2002
                E H2 O/MF
L1             39 S E3
L2              1 S TITANIUM/CN
L3            310 S (TI AND N)/ELS AND 2/ELC.SUB
L4              1 S ALUMINIUM/CN

     FILE 'HCAPLUS' ENTERED AT 08:03:14 ON 28 JUN 2002
L5         456567 S ELECTRODE
L6           1763 S FERROELECTRIC()CAPACITOR
L7         205781 S TITANIUM()NITRIDE OR TI()N OR TIN
L8         467757 S TI OR TITANIUM
L9        1171208 S AL OR ALUMINUM
L10          8432 S (WIR### OR LIN###)(W)(LAYER OR FILM OR COAT####)
L11         84293 S CVD OR (CHEMICAL OR CHEM)(2N)(VAPOUR OR VAPOR)(2N)DEPOSIT? OR
L12        812002 S CONDUCT######
L13        240218 S INFILTRAT? OR PENETRAT? OR PERMEAT?
L14           977 S  L5 AND L6
                E SPUTTER?/CT
                E E7+ALL/CT
                E E10-20
                E SPUTTER?/CT
                E E7+ALL/CT
L15         52831 S E10-20
L16          7603 S TIN()(SPUTTER? OR L15)
L17          7603 S TIN(W)(SPUTTER? OR L15)
L18         25268 S TITANIUM()NITRIDE
L19          8715 S (L18 OR TIN)(W)(SPUTTER? OR L15)
L20             5 S L14 AND L10
L21            16 S L14 AND L13
L22            16 S L21 NOT L20
L23             0 S L14 AND REDUC###()AGENT
L24            11 S L14 AND L2 AND L3 AND L4 AND L7 AND L8 AND L9
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L29            18 S L28 AND L15
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L31            13 S L29 NOT (L24 OR L21 OR L20 OR 27)
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L33             5 S L32 NOT (L24 OR L21 OR L20 OR L27 OR L30)
L34            12 S L30 NOT (L24 OR L21 OR L20 OR L27 OR L29)
L35             9 S TIN()SPUTTER? AND L11
L36             9 S L35 NOT (L24 OR L21 OR L20 OR L27 OR L29 OR L30)
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L20 ANSWER 1 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:366662 HCAPLUS
TI Novel Pb(Ti,Zr)O3(PZT) crystallization technique using flash lamp for ferroelectric RAM (FeRAM) embedded LSIs and one transistor type FeRAM devices
AU Yamakawa, Koji; Imai, Keitaro; Arisumi, Osamu; Arikado, Tsunetoshi; Yoshioka, Masaki; Owada, Tatsushi; Okumura, Katsuya
CS Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corp., Yokohama, 235-8522, Japan
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (2002), 41(4B), 2630-2634
CODEN: JAPNDE
PB Japan Society of Applied Physics
DT Journal
LA English
AB A novel method of **ferroelec. capacitor** formation for Ferroelectrie random access memory (FeRAM) embedded LSIs and one-transistor-type FeRAMs has been developed. Amorphous Pb(Ti,Zr)O3(PZT) films were successfully transformed to the perovskite phase by a flash lamp technique with a crystn. time of 1.2 ms at a substrate temp. of 350.degree.C. A flash lamp energy of 27 J/cm2 was sufficient to form a ferroelec. crystal structure due to rapid thermal effects with little heat diffusion in the depth direction. This technique enabled PZT film crystn. in Pt/PZT/Pt structures on multi-Al **wiring layers**. Granular PZT grains were obsd. on Pt, Ru and RuO2 **electrodes**, which indicates that crystal growth begins from the film surfaces. Ferroelec. property was verified by the process at 350.degree.C max. temp. PZT films were also crystd. directly on SiO2. This is useful for the fabrication of embedded FeRAM devices and 1Tr-type FeRAMs. The flash lamp process was found to have great potential for application to dielec. film formation, annealing processes and so on.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L20 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:727492 HCAPLUS
TI Ferroelectric memory and its production method. [Machine Translation].
IN Ozaki, Toru
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001274350	A2	20011005	JP 2000-87388	20000327
	US 2002000585	A1	20020103	US 2001-816245	20010326
PRAI	JP 2000-87388	A	20000327		

AB [Machine Translation of Descriptors]. The ferroelectric memory where retrieval annealing after wiring contact opening becomes possible, can actualize satisfactory **ferroelectric capacitor** quality is offered. The source of the plural memory cell transistors and the aforementioned memory cell transistor which were formed on the semiconductor substrate / the plug **electrode** which is provided in the form which contacts the drain territory respectively and the

ferroelectric capacitor and the aforementioned source of the sandwich laminate structure which provides the ferroelectric membrane with the source / the 1st lower part **electrode** and the upper **electrode** of the aforementioned memory cell transistor which was formed on the plug **electrode** of one side of the drain territory / had with the **wiring layer** which connects with the 2nd lower part **electrode** and the aforementioned upper **electrode** and the aforementioned 2nd lower part **electrode** which were formed to the top of the plug **electrode** where the drain territory is connected on the other hand.

L20 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:713791 HCAPLUS
DN 135:250483
TI Method of manufacturing a **ferroelectric capacitor** with minimization of hydrogen degradation
IN Lee, June-key; Koo, Bon-jae
PA S. Korea
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001023951	A1	20010927	US 2001-816216	20010326
	JP 2001284549	A2	20011012	JP 2001-32359	20010208
PRAI	KR 2000-15033	A	20000324		
	KR 2000-86285	A	20001229		

AB A method of manufg. a **ferroelec. capacitor** includes the steps of forming a lower **electrode** on a substrate, forming a ferroelec. layer on the lower **electrode**, forming an upper **electrode** on the ferroelec. layer, forming a **wiring layer** on the upper **electrode**, and applying a voltage to an **electrode** selected from the upper **electrode** and the lower **electrode**, the voltage being greater than the operational voltage of the **electrode**, to regularly align an elec. dipole of the ferroelec. layer.

L20 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:399254 HCAPLUS
DN 133:36790
TI Fabrication of semiconductor ferroelectric RAM memory devices in decreased contact resistance
IN Takahashi, Seiichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000164827	A2	20000616	JP 1998-334247	19981125
	JP 3144405	B2	20010312		

AB The title fabrication involves (1) prepg. a FET on a semiconductor substrate, (2) forming a 1st insulator film over the entire surface, (3) providing a lower **electrode**, capacitance insulator film, and an

upper **electrode** to give a capacitor on the 1st insulator film, (4) forming a 2nd insulator film over the entire surface, (5) opening a 1st contact hole to the 2nd insulator film to expose the upper **electrode**, (6) annealing the capacitor in an oxidative atm., (7) depositing a metal silicide film over the entire surface, (8) opening 2nd contact holes to the silicide/2nd-insulator/1st-insulator multilayers to expose the source/drain diffusion layers and gate **electrode**, and (9) forming a metal circuit **wire layer** which is connected to the source/drain diffusion layers and gate **electrode** via the contact holes. The arrangement of the 2nd contact holes prevents unwanted diffusion of dopants into the metal silicide layer from the diffusion layers during annealing and consequently eliminates deterioration of the **ferroelec. capacitors** and increase of the contact resistance. in the diffusion layers.

L20 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:574935 HCAPLUS
DN 127:256294
TI **Ferroelectric capacitor**, wiring, semiconductor device and thir production methods.
IN Fukuda, Yukio; Aoki, Katsuhiro; Numata, Inui
PA Texas Instruments Japan Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 09223779	A2	19970826	JP 1996-54140	19960216

AB A **ferroelec. capacitor** formed on an insulator layer comprises a ferroelec. film having a top **electrode** and a bottom **electrode** which has a bottom layer contg. a material for reducing the insulator layer to improve the bonding strength between the bottom **electrode** and the insulator layer. Specifically, the bottom layer of the bottom **electrode** may comprise Ti or Al, and the top layer of the top **electrode** may comprise Pt, Ir, Ru, Pd, Ag, or Au. A **wiring layer** formed on the insulator layer is also described, which contains a material for reducing the insulator layer. A semiconductor device, esp. a nonvolatile memory, is also described, which comprises the above capacitor and wiring.

L22 ANSWER 1 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:466467 HCAPLUS
TI **Ferroelectric capacitors** for integrated circuit memory devices and methods of manufacturing same
IN Lee, Kyu-mann
PA S. Korea
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2002074588	A1	20020620	US 2001-900269	20010706
PRAI KR 2000-79189	A	20001220		

AB Methods of forming integrated circuit capacitors having dielec. layers therein that comprise ferroelec. materials, include the use of protective layers to block the **infiltration** of hydrogen into the ferroelec. material. By blocking the **infiltration** of hydrogen, the hysteresis characteristics of the ferroelec. materials can be preserved. A preferred integrated circuit capacitor comprises a semiconductor substrate and a lower capacitor **electrode** on the semiconductor substrate. A capacitor dielec. layer that comprises a ferroelec. material, is provided on the lower capacitor **electrode**. An upper capacitor **electrode** is also provided on the capacitor dielec. layer. In order to inhibit degrdn. of the ferroelec. characteristics of the capacitor dielec. layer, a protective layer is utilized to cover the capacitor dielec. layer. In particular, the protective layer is formed to encapsulate the upper capacitor **electrode** and the capacitor dielec. layer. The protective layer preferably includes a material that is substantially free of hydrogen and has a chem. and/or phys. structure that blocks transfer (e.g., diffusion) of hydrogen therethrough. The protective layer may also have a thickness of greater than about 50 .ANG., in order to further inhibit transfer of hydrogen from outside the protective layer to the underlying capacitor dielec. layer. The protective layer may comprise a metal oxide selected from the group consisting of Al2O3, TiO2, SiO2, ZrO2 and CeO2.

L22 ANSWER 2 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:273249 HCAPLUS
DN 136:317753
TI Ferroelectric memory devices
IN Yoshikawa, Takafumi; Mikawa, Takumi; Hayashi, Shinichiro
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2002110931	A2	20020412	JP 2000-302215	20001002

AB **Ferroelec. capacitors** are formed on substrates, and the top capacitor **electrodes**, or the **electrodes** as well as their sidewalls and those of **ferroelec. capacitor** films are covered with TiAl or its nitride films that have barrier characteristic against elec. conductive H2. Deterioration of

the capacitors by H **infiltration** is prevented.

L22 ANSWER 3 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:158230 HCAPLUS
DN 136:209285
TI Method of manufacturing semiconductor device including **ferroelectric capacitor** Ir/IrO2/Pt/PZT/Pt/IrO2/Ir
IN Jung, Dong-Jin; Kim, Ki-Nam
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002024074	A1	20020228	US 2001-924206	20010807
PRAI	KR 2000-49623	A	20000825		

AB A semiconductor device using a triple layered structure of metal layer/metal oxide layer/metal layer as an **electrode** of a capacitor is provided. According to the manufg. method, a conductive plug elec. connected to a semiconductor substrate is formed by **penetrating** through a 1st insulating layer on the semiconductor substrate. An adhesive layer is formed on the conductive plug to form a 1st lower metal layer made of noble metals such as Ir that is elec. connected to the conductive plug and prevents diffusion of O into the conductive plug on the 1st insulating layer. A conductive lower metal oxide layer is formed on the 1st lower metal layer, and a 2nd lower metal layer for inducing interface lattice matching is preferably formed of Pt to form a lower **electrode** layer of a capacitor. A ferroelec. layer is formed of a ferroelec. material such as Pb(Zr1-xTix)O3 (PZT) on the lower **electrode** layer of a capacitor. A 1st upper metal layer for inducing interface lattice matching is formed on top of the ferroelec. layer, and a heat treatment is performed above the crystn. temp. of the ferroelec. material to induce interface lattice matching. Then, an upper metal oxide layer may be formed noble metal oxides such as Ir oxide on top of the 1st upper metal layer, and then a 2nd upper metal layer for preventing diffusion of a material is formed of noble metals such as Ir on top of the upper metal oxide layer to form an upper **electrode** layer. A 2nd insulating layer is formed on the upper **electrode** layer and the 2nd insulating layer is patterned to form a wire therein elec. connected to the upper **electrode** layer.

L22 ANSWER 4 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:139192 HCAPLUS
DN 136:192743
TI Manufacture of semiconductor memory cells containing **ferroelectric capacitors**
IN Watabe, Hiroshi; Nishina, Eiichi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002057297	A2	20020222	JP 2000-239428	20000808

AB After forming top **electrodes** on the ferroelec. films (e.g., Bi2SrTa2O9) which are in turn formed on bottom **electrodes**, the laminates are heat treated in inactive atm. contg. small amt. of oxidative gases. Atoms in the ferroelec. films are prevented from **infiltration** into and reaching the top of the top **electrodes**.

L22 ANSWER 5 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:912598 HCAPLUS
DN 136:176270
TI Mechanism for hydrogen damage in ferroelectric Pt/Bi4-xLaxTi3O12/Pt capacitors during FGA process
AU Chon, U.; Cho, M. K.; Hong, G. G.; Lee, S. K.; Kim, S. U.; Park, B. H.
CS RIST, S. Korea
SO RIST Yongu Nonmun (2001), 15(3), 340-344
CODEN: RYNOEQ; ISSN: 1225-486X
PB Research Institute of Industrial Science & Technology
DT Journal
LA English
AB Degrdn. mechanism of ferroelec. properties in the Pt/Bi4-xLaxTi3O12/Pt (Pt/BLT/Pt) film capacitors during forming gas annealing (FGA) was systematically studied by examg. ferroelec. responses, elec. resistivities and spatial distributions of relevant species using SIMS. The degrdn. of ferroelec./elec. properties in the Pt/BLT/Pt capacitor during FGA was not originated from the O loss induced by a reducing atm. but was mainly caused by protons and electrons catalytically dissocd. from H2 by the top Pt **electrode**. The following sequential mechanism was identified from the present study: (i) the adsorption and dissocn. of H2 to produce protons and electrons by the top Pt **electrode**, (ii) the columnar **penetration** of protons into the BLT film, accelerated by the region of neg. charged Bi-site vacancies near the bottom **electrode**, and (iii) the decompn. of perovskite phase into paraelec. (Bi,La)2Ti2O7 and Ti6O11 after FGA at 400.degree..
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 6 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:740236 HCAPLUS
DN 136:30164
TI Degradation mechanism of ferroelectric properties in Pt/Bi4-xLaxTi3O12/Pt capacitors during forming gas annealing
AU Chon, Uong; Kim, Ki-Bum; Jang, Hyun M.
CS Department of Materials Science and Engineering, and National Research Laboratory (NRL) for Ferroelecric Phase Transitions, Pohang University of Science and Technology (POSTECH), Pohang, 790-784, S. Korea
SO Applied Physics Letters (2001), 79(15), 2450-2452
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB Degrdn. mechanism of ferroelec. properties in the Pt/Bi3.15La0.85Ti3O12/Pt (Pt/BLT/Pt) capacitors during forming gas annealing (FGA) was systematically studied by examg. ferroelec. responses and spatial distributions of relevant species using secondary ion mass spectrometry. The degrdn. of ferroelec. properties during FGA was not originated from the O loss induced by a reducing atm. but was mainly caused by protons catalytically dissocd. from H2 by the top Pt **electrode**. The following sequential mechanism was identified from the present study: (i)

the adsorption and dissocn. of H2 to produce protons and electrons by the top Pt **electrode**, (ii) the columnar **penetration** of protons into the BLT film, accelerated by the region of neg. charged Bi-site vacancies near the bottom **electrode**, and (iii) the decompn. of perovskite phase after FGA at 400.degree..
RE.CNT 22 THERE ARE 22 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 7 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:710271 HCAPLUS
DN 135:265792
TI **Ferroelectric capacitor** memory devices and fabrication for increased residual polarization in ferroelectric layers
IN Kodaka, Yasutoshi; Goto, Yasuyuki; Otani, Shigemoto; Ashida, Hiroshi
PA Fujitsu Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2001267519	A2	20010928	JP 2000-76907	20000317

PI JP 2001267519 A2 20010928 JP 2000-76907 20000317
AB The title fabrication involves (1) forming on a substrate with a capacitance ferroelec. layer contg. a 1st metal, (2) forming an upper **electrode** layer on the ferroelec. layer, (3) reductive 1st annealing of the ferroelec./**electrode** layers to diffuse the 1st metal from the ferroelec. layer into the upper **electrode** layer, and (4) oxidative 2nd annealing the layers to recover the ferroelec. characteristics which are lost by redn. The 1st metal-diffused region in the upper **electrode** becomes more H-absorbing or less H-**permeating** to protect the ferroelec. capacitance layer against further hydrogen redn. or reductive ferroelec. deterioration.

L22 ANSWER 8 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:449009 HCAPLUS
DN 133:158401
TI Protection of SrBi2Ta2O9 **ferroelectric capacitors** from hydrogen damage by optimized metallization for memory applications
AU Hong, Suk-Kyoung; Suh, Chung Won; Lee, Chang Goo; Lee, Seok Won; Kang, Eung Youl; Kang, Nam Soo; Hwang, Cheol Seong; Kwon, Oh Seong
CS FeRAM Team, Memory R&D Division, Hyundai Electronics Industries Company Ltd., Ichon-si, Kyoungki-do, 467-701, S. Korea
SO Applied Physics Letters (2000), 77(1), 76-78
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB The degrdn. behavior of integrated Pt/SrBi2Ta2O9/Pt capacitors by hydrogen impregnation during the intermetal dielec. deposition and passivation is investigated. The hydrogen ions generated as a reaction byproduct from the SiH4-based deposition processes of the dielec. films induce redn. in the remanent polarization (Pr) as well as the imprint behavior of the small size capacitors (2.times.2 .mu.m2). The degree of degrdn. is quite dependent on the size of the individual capacitors. The smaller capacitors underwent more serious degrdn. implying that the hydrogen ions impregnate into the SBT layer mainly along the etched side area of the capacitors not through the top Pt **electrode**. Metalization

adopting TiN/Al/TiN/Ti multilayers is very effective in suppressing the hydrogen impregnation. In particular, the Ti layer appears to block the hydrogen **penetration**. Therefore, the optimized metalization scheme, wider metal lines than the top **electrode** area by 1 .mu.m, successfully protects the integrated capacitors from hydrogen damage. 12 .mu.C/cm2 of 2Pr and 1.1 V of 2Vc (coercive voltage) with an imprinting voltage of 0.16 V were obtained from the passivated 2.times.2 .mu.m2 array capacitors by the optimized metalization.

RE.CNT 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 9 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:383827 HCAPLUS
DN 133:11765
TI Semiconductor memory device having a hydrogen barrier layer, and method for manufacturing the same
IN Nagano, Yoshihisa; Tanaka, Keisuke; Nasu, Toru
PA Matsushita Electronics Corporation, Japan
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1006580	A2	20000607	EP 1999-120841	19991025
	EP 1006580	A3	20010620		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	TW 434877	B	20010516	TW 1999-88118140	19991020
	CN 1257311	A	20000621	CN 1999-122843	19991130
	KR 2000047773	A	20000725	KR 1999-53695	19991130
	US 6326671	B1	20011204	US 1999-452620	19991201
	JP 2000228499	A2	20000815	JP 1999-343912	19991202
	CN 1257310	A	20000621	CN 1999-127744	19991203
PRAI	JP 1998-343896	A	19981203		

AB A semiconductor memory device which comprises a 1st protective insulation film 3 covering the whole surface of a semiconductor substrate having a transistor composed of a source region, a drain region and a gate integrated thereon, a capacitative element for data storage composed of a lower **electrode** 4, a capacitative film 5 of an insulating metal oxide and an upper **electrode** 6 formed on the 1st protective insulation film 3, a 2nd protective insulation film 7 covering the whole surface of 1st protective insulation film 3 and the capacitative elements, a H barrier layer 10, 11 formed to cover the whole surfaces of contact holes 8, 9 formed through the 2nd protective insulation film 7 **penetrating** resp. to the upper **electrode** 6 and the lower **electrode** 4 and the exposed surfaces of upper **electrode** 6 and lower **electrode** 4, a contact hole 12 formed through the 1st protective insulation film 3 and the 2nd protective insulation film 7 **penetrating** to the transistor, and an interconnection layer 13 which elec. connects the capacitative element and the transistor. In the memory device, the catalytic reaction against H, which takes place at the surfaces of upper **electrode** and the lower **electrode** during resist removal with O plasma, can be suppressed. Thus, a semiconductor memory device contg. capacitative elements of high reliability is presented.

L22 ANSWER 10 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:89665 HCAPLUS
DN 132:145367
TI Semiconductor device and its manufacture
IN Kanay, Hiroyuki; Kunishima, Iwao; Yamakawa, Koji
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000040799	A2	20000208	JP 1998-208999	19980724
	US 2002063274	A1	20020530	US 1999-359324	19990723
PRAI	JP 1998-208999	A	19980724		
	JP 1998-324254	A	19981113		
	JP 1998-345368	A	19981204		

AB The semiconductor device has a **ferroelec. capacitor** composed of (A) a lower **electrode**, (B) two polycryst. ferroelec. films (1) which have different grain size each other or (2) both of which are composed of the same perovskite compds. to form a crystal grain boundary at their interface, and (C) an upper **electrode**. The semiconductor device has a difusion layer between the ferroelec. layer and both of upper and lower **electrodes**, resp. The device is manufd. by (1) forming a lower **electrode** on a semiconductor substrate via an elec. insulating layer, (2) forming a ferroelec. layer on the upper **electrode** film, (3) annealing the ferroelec. layer to crystallize it, (4) forming another ferroelec. layer on the crystd. ferroelec. layer, (5) forming an upper **electrode** film on the ferroelec. layer, and (6) crystg. the latter ferroelec. layer. The device shows less damage of the capacitor layer because of less H **penetration** to improve reliability.

L22 ANSWER 11 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:40056 HCAPLUS
DN 130:118219
TI Ferroelectric memory devices
IN Tanabe, Nobuhiro
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11008355	A2	19990112	JP 1997-158556	19970616

AB H2 barrier films are formed on the top **electrodes** of **ferroelec. capacitors**, and elec. conductive and insulating H2 barriers are formed under the bottom **electrodes**, where the bottom **electrodes** are connected with contact plugs across the H2 barrier films. Deterioration of **ferroelec. capacitors** due to H2 **infiltration** is prevented.

L22 ANSWER 12 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:494148 HCAPLUS
DN 127:228196

TI Barrier properties for oxygen diffusion in a TaSiN layer
AU Hara, Tohru; Tanaka, Masaru; Sakiyama, Keizo; Onishi, Shigeo; Ishihara, Kazuya; Kudo, Jun
CS Electrical Engineering, Hosei University, Koganei, 184, Japan
SO Japanese Journal of Applied Physics, Part 2: Letters (1997), 36(7B), L893-L895
CODEN: JAPLD8; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB Annealing in O2 at temps. above 650.degree.C is required for a thin **ferroelec. capacitor**. Redn. of the leakage current and an increase of capacitance can be attained in the charge storage capacitor through this annealing. A stacked structure capacitor cell must be practically employed in metal oxide semiconductor large scale integrated circuits (MOSLSI). In this capacitor cell with a conventional Pt/TiN/poly-Si lower **electrode**, however, O2 annealing can not be attained at high temp. because peeling of the TiN barrier layer and the formation of a thin oxide layer at the surface of poly-Si occur. An noncryst. TaSiN layer has been studied with respect to the barrier effect for oxygen diffusion used in the barrier layer of the lower **electrode**. The **penetration** depth of oxygen diffusion decreases markedly with increasing Si compn. in a TaSiN layer and reaches 20 nm deep in a Ta.22Si.35N.43 layer. However, the resistivity increases with this increase. A good diffusion barrier layer with low sheet resistance is attained in a Ta.50Si.16N.34 layer. **Penetration** depth below 40 nm is obtained in a slightly Si-rich Ta.36Si.27N.37 layer for O2 annealing at 850.degree.C.

L22 ANSWER 13 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:233430 HCAPLUS
DN 126:324147
TI Barrier effect for the O diffusion in TaSiN **electrode** employed in charge storage capacitor
AU Kobayashi, Takuya; Tanaka, Masaru; Hara, Tohru
CS Electrical Engineering, Hosei University, Koganei, 184, Japan
SO Report of Research Center of Ion Beam Technology, Hosei University, Supplement (1997), 15, 87-90
CODEN: RCISDS; ISSN: 0914-2908
PB Hosei Daigaku Ion Bimu Kogaku Kenkyusho
DT Journal
LA English
AB Barrier properties for O diffusion were studied for Ta Si nitride layers of different compns. The O **penetration** depth at 650.degree. decreases and the resistance increases as the Si content increases. The optimum compn. is Ta0.36Si0.27N0.37. This barrier layer can be used for **ferroelec. capacitors** from SrBi2Ta2O9.

L22 ANSWER 14 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:216118 HCAPLUS
DN 126:271086
TI **Electrode** structure for **ferroelectric capacitors** in integrated circuits
IN Chivukula, Vasanta; Leung, Pak K.
PA Northern Telecom Limited, Can.
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent

LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5612560	A	19970318	US 1995-551264	19951031
	US 5789268	A	19980804	US 1996-728373	19961010
PRAI	US 1995-551264		19951031		

AB An improved **electrode** structure compatible with **ferroelec**. **capacitor** dielecs. is provided. In particular, a multilayer **electrode** having improved adhesion to ferroelec. materials such as PZT is formed, comprising a 1st layer of a noble metal, a 2nd layer of another metal, and a thicker layer of the noble metal, which are annealed to cause controlled interdiffusion of the layers, forming a mixed metal surface layer having a rough interface with the dielec. layer. E.g., the 1st 2 layers comprise relatively thin (.apprx.200 .ANG.) layers of Pt and Ti, and then a thicker layer of the main, 1st, **electrode** material is deposited on top. Nonuniform interdiffusion of the layers during annealing causes intermixing of the Pt and Ti layers at the interfaces, forming a Pt/Ti alloy having a rough surface. The rough surface, and particularly hillocks formed at the interface, **penetrate** into the ferroelec. films, and anchor the **electrode** material to the dielec. Improved adhesion of the conductive **electrode** material improves the integrity of this interface during subsequent processing.

L22 ANSWER 15 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:165302 HCAPLUS
DN 126:165303
TI Barrier layer for a **ferroelectric capacitor** integrated on silicon
IN Ramesh, Ramamoorthy
PA Bell Communication Research, Inc., USA
SO PCT Int. Appl., 25 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9701854	A1	19970116	WO 1996-US10780	19960624
	W: CA, CN, JP, KR, MX, PL, SG				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	CA 2225681	AA	19970116	CA 1996-2225681	19960624
	JP 11502376	T2	19990223	JP 1996-504500	19960624
	EP 972309	A1	20000119	EP 1996-923401	19960624
	R: DE, FR, GB, NL, SE				
	IL 118756	A1	20001121	IL 1996-118756	19960628
	US 5838035	A	19981117	US 1997-896508	19970610
PRAI	US 1995-497457	A	19950628		
	WO 1996-US10780	W	19960624		

AB In a ferroelec. memory cell, a ferroelec. stack of a perovskite ferroelec. sandwiched by cubic perovskite metal oxide conductive **electrodes** is formed over a Si body, such as a polysilicon plug **penetrating** a field oxide over a Si transistor. An oxidn. barrier is placed between the lower metal oxide **electrode** and the polysilicon. The oxidn. barrier may be: a refractory metal sandwiched between 2 Pt layers which forms a refractory oxide in a Pt matrix; an intermetallic barrier beneath a Pt **electrode**, e.g., of NiAl; or a combination of Ru and SrRuO3

or similar materials. Thereby, the polysilicon plug is protected from oxidn.

L22 ANSWER 16 OF 16 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:97426 HCAPLUS
DN 116:97426
TI Manufacture of semiconductor devices containing ferroelectric materials
IN Takenaka, Kazuhiro
PA Seiko Epson Corp., Japan
SO PCT Int. Appl., 24 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9116731	A1	19911031	WO 1991-JP539	19910423
	W: JP, KR, US				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, NL, SE				
	EP 478799	A1	19920408	EP 1991-908469	19910423
	EP 478799	B1	19961204		
	R: DE, FR, GB, IT, NL				
	JP 3003049	B2	20000124	JP 1991-507551	19910423
	US 5293510	A	19940308	US 1991-778895	19911220
PRAI	JP 1990-108011	A	19900424		
	JP 1990-108012	A	19900424		
	JP 1990-108013	A	19900424		
	WO 1991-JP539	W	19910423		

AB A semiconductor device contains, in a source region between a gate **electrode** and a local oxide film, a **ferroelec. capacitor** which comprises a top and a bottom **electrode** and a ferroelec. film in between, and has an elec.-conductive oxide film (composed of In-Sn-O, ReO2, RuO2, and/or MoO3) between the bottom **electrode** and the source region. In order to improve crystallinity of the ferroelec. film, it is annealed with O. Though O **infiltrates** into the elec.-conductive oxide film to some extent, no adverse effect is caused except further oxidn. of the oxide film. This is because the oxide film serves as a barrier to oxidn. or a dummy layer, so that Si at the interface with the source is substantially protected from oxidn. Therefore, decrease in contact resistance and development of series parasitic capacitance are avoided to increase freedom of forming the capacitor region, and to increase the degree of integration.

L25 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:84625 HCAPLUS
DN 136:143863
TI Confinement of E-fields in high density ferroelectric memory device structures
IN Van Buskirk, Peter C.; Bilodeau, Steven M.
PA Advanced Technology Materials, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6342711	B1	20020129	US 1999-264047	19990308
	US 2001035543	A1	20011101	US 2001-893155	20010627
PRAI	US 1999-264047	A1	19990308		

AB A **ferroelec. capacitor** device structure, including a ferroelec. stack capacitor comprising a ferroelec. material capacitor element on a substrate contg. buried transistor circuitry beneath an insulator layer having a via therein contg. a conductive plug to the transistor circuitry, in which E-fields are structurally confined to the **ferroelec. capacitor** material element. Such E-fields confinement may be effected by fabrication of the device structure including: (a) patterning the stack capacitor, and depositing a non-ferroelec., high .epsilon. material layer over and on the sides of the stack capacitor; (b) forming the stack capacitor without patterning the ferroelec. material and rendering a portion of the material non-ferroelec. in character; or (c) forming the ferroelec. stack capacitor with an aspect ratio, of effective lateral dimension d of the **ferroelec. capacitor** material element to thickness t of the **ferroelec. capacitor** material element, that is >5, with d and t being measured in same dimensional units.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:781432 HCAPLUS
DN 135:337834
TI Hardmask designs for dry etching FERAM capacitor stacks
IN Moise, Theodore; Gilbert, Stephen R.; Summerfelt, Scott R.; Xing, Guoqiang; Colombo, Luigi
PA USA
SO U.S. Pat. Appl. Publ., 22 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001034106	A1	20011025	US 2000-741479	20001219
PRAI	US 1999-171794P	P	19991222		

AB An embodiment of the instant invention is a **ferroelec. capacitor** formed over a semiconductor substrate, the **ferroelec. capacitor** comprising: a bottom **electrode** formed over the semiconductor substrate, the bottom **electrode** comprised of a bottom **electrode** material; a

top **electrode** formed over the bottom **electrode** and comprised of a 1st **electrode** material; a ferroelec. material situated between the top **electrode** and the bottom **electrode**; and a hardmask formed on the top **electrode** and comprising a bottom hardmask layer and a top hardmask layer formed on the bottom hardmask layer, the top hardmask layer able to with stand etchants used to etch the bottom **electrode**, the top **electrode**, and the ferroelec. material to leave the bottom hardmask layer substantially unremoved during the etch and the bottom hardmask layer being comprised of a conductive material which substantially acts as a H2 diffusion barrier.

L25 ANSWER 3 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:703060 HCAPLUS
DN 135:250337
TI Ferroelectric memory devices including capacitors located outside the active area and made with diffusion barrier layers
IN Jung, Dong-Jin
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6294805	B1	20010925	US 1997-869704	19970605
	JP 10056143	A2	19980224	JP 1997-146675	19970604
	US 2002004248	A1	20020110	US 1998-52718	19980331
	US 6359295	B2	20020319		
	JP 11111933	A2	19990423	JP 1998-156466	19980604
PRAI	KR 1996-20359	A	19960607		
	US 1997-869704	A	19970605		
	KR 1997-49758	A	19970929		

AB Integrated circuit ferroelec. memory devices include a pair of spaced apart word lines which cross an elongated active region, a drain region in the active region between the pair of word lines, and a pair of source regions in the active region outside the pair of spaced apart word lines on opposite sides of the drain region. A pair of **ferroelec. capacitors** outside the elongated active region is also included, a resp. 1 of which is adjacent a resp. 1 of the pair of source regions. Each of the **ferroelec. capacitors** includes spaced apart 1st and 2nd **electrodes** and a ferroelec. layer between them. A resp. 1 of the 1st **electrodes** is elec. connected to a resp. 1 of the pair of source regions. A pair of plate lines is elec. connected to a resp. 1 of the 2nd **electrodes** and a bit line is elec. connected to the drain region. Integrated circuit ferroelec. memory devices according to the invention may be formed by fabricating a field effect transistor in an integrated circuit substrate and forming a 1st **electrode**, a ferroelec. layer, a diffusion barrier layer and a 2nd **electrode** on the substrate. A 1st patterned metal layer elec. connects the 1st **electrode** to the source region of the field effect transistor and also elec. contacts the drain region. A 2nd patterned metal layer elec. contacts the 2nd **electrode**.

RE.CNT 24 THERE ARE 24 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:362724 HCAPLUS
DN 135:85229
TI Low thermal-budget fabrication of sputtered-PZT capacitor on multilevel interconnects for embedded FeRAM
AU Inoue, Naoya; Nakura, Takeshi; Hayashi, Yoshihiro
CS NEC, Sagamihara, 229-1198, Japan
SO Technical Digest - International Electron Devices Meeting (2000) 797-800
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Low temp. fabrication of the PZT capacitor is achieved by O2-free sputtering on the O-doped Ir (Ir(O)). O gas stabilizes the nonferroelec. pyrochlore phase, therefore O2-free PZT sputtering enforces the deposition of ferroelec. perovskite phase. The Ir(O) bottom **electrode**, in which the O atoms are fixed in the Ir-lattice, also helps the direct deposition of the perovskite PZT even at 450.degree.-475.degree.. This low thermal-budget process enables the authors to fabricate the PZT capacitor on the multilevel **Al**-interconnects for the FeRAM-embedded logic LSI.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 5 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:258951 HCAPLUS
DN 135:12847
TI Fabrication of double metal FeRAM without degradation of remnant polarization by using Ir/IrOx capacitor contact barrier layer
AU Kweon, Soon Yong; Yeom, Seung Jin; Lee, Sahang Kyoo; Yu, Yong Sik; Pyun, Deuk Soo; Kim, Cheong Tae
CS Memory Research and Development Division, Hyundai Electronics Industries Co. Ltd., Kyungki-do, 467-860, S. Korea
SO Integrated Ferroelectrics (2000), 31(1-4), 251-259
CODEN: IFEREU; ISSN: 1058-4587
PB Gordon & Breach Science Publishers
DT Journal
LA English
AB The capacitor contact barrier (CCB) structure was introduced to prevent both the Pt/**Al** reaction and the **Ti** effect to a SBT capacitor. **TiN** CCB layer could not perfectly block the Pt/**Al** reaction. And ferroelec. properties of SBT capacitor were degraded during back-end processes. So, the authors applied a new Ir/IrOx layer to the CCB layer. The SBT capacitor with the Ir/IrOx CCB layer exhibited higher delta polarization (dP.apprx.15 .mu.C/cm2) after the metal-2 etching process, compared with the value in the case of the **TiN** CCB layer (dp.apprx.12.mu.C/ cm2). Also, the dP uniformity was improved to 4% when the authors used the Ir/IrOx CCB layer, from the .apprx.20% of the **TiN** CCB layer. And the defect formed by the Pt/**Al** reaction was not found in the Ir/IrOx CCB layer structure.
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:241803 HCAPLUS
DN 134:246271
TI Completely encapsulated top **electrode** of a **ferroelectric capacitor** using a lead-enhanced encapsulation layer
IN Eastep, Brian Lee; Evans, Thomas A.

PA Ramtron International Corporation, USA
SO U.S., 27 pp., Cont.-in-part of U.S. 6,027,947.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6211542	B1	20010403	US 1998-85280	19980527
	US 5920453	A	19990706	US 1996-700076	19960820
	US 5864932	A	19990202	US 1996-728740	19961011
	US 6027947	A	20000222	US 1997-828157	19970327
	US 2001001488	A1	20010524	US 2001-759128	20010111
	US 6281023	B2	20010828		
PRAI	US 1996-700076	A2	19960820		
	US 1996-728740	A2	19961011		
	US 1997-828157	A2	19970327		
	US 1998-85280	A3	19980527		

AB A **ferroelec. capacitor** includes a bottom **electrode**, a top **electrode**, and a ferroelec. layer located between the top and bottom **electrodes** that extends to completely encapsulate the top **electrode**, except for a contact hole to allow metalization of the top **electrode**. The total encapsulation of the top **electrode** reduces the sensitivity of the **ferroelec. capacitor** to hydrogen and thus improves elec. switching performance.
RE.CNT 32 THERE ARE 32 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 7 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:100864 HCAPLUS
DN 134:156555
TI Fabrication of ferroelectric memory devices in prevention of stress-caused deterioration in capacitors
IN Hiroi, Masayuki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001036025	A2	20010209	JP 1999-204713	19990719

AB The title fabrication of the devices in making use of residual polarization characteristics in memory capacitors involves forming a perovskite-type oxide ferroelec. film bound between upper and lower **electrodes**. The fabrication further involves forming a high-thermal-expansion metal circuit such as an **Al** circuit layer over the upper **electrode** by heating at a temp. above the Currie temp. of the ferroelec. oxide film so that the thermal stress mounted on the capacitor from the circuit metal is significantly decreased by heating over the temp. The thermal stress may also be relaxed by using a diffusion barrier film between the upper **electrode** and the circuit layer or by employing a circuit metal having a fluidity at a temp. above the Currie temp.

L25 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:822793 HCAPLUS
DN 133:358240
TI Composite iridium-metal-oxygen barrier structure with refractory metal companion barrier and method for its fabrication for capacitor **electrode** of **ferroelectric capacitors**
IN Zhang, Fengyan; Maa, Jer-Shen; Hsu, Sheng Teng; Zhuang, Wei-Wei
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1054441	A2	20001122	EP 2000-304334	20000522
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	US 6190963	B1	20010220	US 1999-316661	19990521
	JP 2001007298	A2	20010112	JP 2000-149036	20000519
	TW 460930	B	20011021	TW 2000-89109874	20000520
	US 6288420	B1	20010911	US 2000-703192	20001031
PRAI	US 1999-316661	A	19990521		

AB An Ir-M-O composite film was provided that is useful in forming an **electrode** of a **ferroelec. capacitor**, where M includes a variety of refractory metals. The Ir combination film is resistant to high temp. annealing in O environments. When used with an underlying barrier layer made from the same variety of M transition metals, the resulting conductive barrier also suppresses to diffusion of Ir into any underlying Si substrates. As a result, Ir silicide products are not formed, which degrade the **electrode** interface characteristics. That is, the Ir combination film remains conductive, not peeling or forming hillocks, during high temp. annealing processes, even in O. The Ir-M-O conductive **electrode**/barrier structures are useful in nonvolatile FeRAM devices, DRAMs, capacitors, pyroelec. IR sensors, optical displays, optical switches, piezoelec. transducers, and surface acoustic wave devices. A method for forming an Ir-M-O composite film barrier layer and an Ir-M-O composite film ferroelec. **electrode** are also provided.

L25 ANSWER 9 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:227930 HCAPLUS
DN 132:245058
TI Fabrication of a capacitor with a high .epsilon.-dielectric or with a ferroelectric material according to the Fin-Stack principle.
IN Lange, Gerrit; Schloesser, Till; Franosch, Martin; Wendt, Hermann
PA Siemens A.-G., Germany
SO Ger. Offen., 16 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19842682	A1	20000406	DE 1998-19842682	19980917
	TW 437070	B	20010528	TW 1999-88114492	19990824
	JP 2000101046	A2	20000407	JP 1999-260497	19990914
	CN 1254954	A	20000531	CN 1999-120212	19990917
PRAI	DE 1998-19842682	A	19980917		

AB A capacitor with a high .epsilon.-dielec. or **ferroelec.** **capacitor** dielec. and its fabrication method are described. The noble metal storage **electrode** consists of a laminar structure that connects the lamellas to one another. The supporting structure can be constructed to be connected to one or more outer flanks of the lamellas, or they can be arranged inside the lamellas. The fabrication can be done by e.g. a sepn. of the layer sequence with alternating low and high etching rates (if necessary, with an etching stop layer in the lower range), etching until a layer structure is obtained, forming of a supporting structure and selective removal of the layers with higher etching rates.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 10 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:736017 HCAPLUS
DN 128:17864
TI Fabrication of nonvolatile memory device
IN Onishi, Shigeo; Kinoshita, Takao; Kudo, Atsushi
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09293838	A2	19971111	JP 1996-105421	19960425
	US 5854104	A	19981229	US 1997-791406	19970130
PRAI	JP 1996-105421		19960425		

AB The invention relates to a process for making a semiconductor nonvolatile memory device, having a **ferroelec.** **capacitor**, wherein the upper **electrode** of the storage capacitor functions also as the driver line.

L27 ANSWER 1 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:216196 HCAPLUS
DN 136:255863
TI Method of manufacturing semiconductor device comprising a capacitor
IN Hikosaka, Yukinobu; Ozaki, Yasutaka; Takai, Kazuaki
PA Fujitsu Limited, Japan
SO Eur. Pat. Appl., 40 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1189262	A2	20020320	EP 2001-302891	20010328
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2002094021	A2	20020329	JP 2000-282730	20000918
	US 2002061620	A1	20020523	US 2001-819738	20010329
PRAI	JP 2000-282730	A	20000918		

AB There is provided a semiconductor device which comprises a capacitor including a lower **electrode**, a dielec. film, and an upper **electrode**, a 1st protection film formed on the capacitor, a 1st wiring formed on the 1st protection film, a 1st insulating film formed on the 1st wiring, a 2nd wiring formed on the 1st insulating film, a 2nd insulating film formed on the 2nd wiring, and .gtoreq.1 of a 2nd protection film formed between the 1st insulating film and the 1st wiring to cover at least the capacitor and a 3rd protection film formed on the 2nd insulating film to cover the capacitor and set to an earth potential. Accordingly, the degrdn. of the **ferroelec. capacitor** formed under the multi-layered wiring structure can be suppressed.

L27 ANSWER 2 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:876419 HCAPLUS
DN 136:176257
TI Demonstration of scaled (.gtoreq.0.12 .mu.m2) Pb(Zr,**Ti**)O3 capacitors on W plugs with **Al** interconnect
AU Summerfelt, S. R.; Moise, T. S.; Xing, G.; Colombo, L.; Sakoda, T.; Gilbert, S. R.; Loke, A. L. S.; Ma, S.; Wills, L. A.; Kavari, R.; Hsu, T.; Amano, J.; Johnson, S. T.; Vestcyk, D. J.; Russell, M. W.; Bilodeau, S. M.; van Buskirk, P.
CS Silicon Technology Development, Texas Instruments Inc., Dallas, TX, 75243, USA
SO Applied Physics Letters (2001), 79(24), 4004-4006
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB The measured switched polarization properties of integrated Pb(Zr, **Ti**)O3 (PZT) capacitors arrays have been found to show a small dependence on individual capacitor size in the range from 0.17 and 100 .mu.m2. These thin (90 nm) PZT capacitors have low voltage switching properties with polarization satn. of <1.8 V with switched polarization for the smallest capacitors (0.17 .mu.m2) still larger than 25 .mu.C/cm2. The capacitor stack consisted of TiAlN hardmask/Ir/IrOx/PZT/Ir/TiAlN on either SiO2 dielec. or W plugs. The capacitor was patterned using 248 nm lithog. and etched using only one mask. For wafers without W plugs, the

Ir bottom **electrode** was not etched. For wafers with W plugs, the entire capacitor stack was etched and elec. connection to the bottom **electrode** was through the W plugs. The capacitors were integrated using SiO2 dielecs. and one level of **Al** metalization. These data suggest that high-d., **ferroelec. capacitor**-based memories may be feasible.

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 3 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:710272 HCAPLUS
DN 135:265593
TI Semiconductor devices having **ferroelectric capacitors** and fabrication of devices thereof
IN Kanetani, Hiroyuki
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001267520	A2	20010928	JP 2000-78916	20000321

AB The title devices comprise a substrate, a diffusion region formed on the substrate, an interlayer insulator film formed on the diffusion region, a contact hole to the insulator film to expose the diffusion region, a contact plug provided in the contact hole and on the insulator film to give a lower **electrode**, a ferroelec. film formed on the lower **electrode**, and an upper **electrode** formed on the ferroelec. film to give a T-shaped **ferroelec. capacitor**. The process provides the fabrication of the **ferroelec. capacitors** with compact shape without employment of capacitor-on-plug structure.

L27 ANSWER 4 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:495389 HCAPLUS
DN 135:101160
TI **Ferroelectric capacitors**
IN Kawakubo, Takashi; Sano, Masaya; Ohara, Ryoichi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001189430	A2	20010710	JP 1999-373063	19991228
	US 2001015448	A1	20010823	US 2000-749788	20001228
PRAI	JP 1999-373063	A	19991228		

AB The bottom **electrodes** of the capacitors, which use BTO (BaTiO3) ferroelec. films, comprise triple layers of (**Ti**, **Al**)N, Ir and SRO (SrRuO3) layers laminated on Si substrates, which have improved wear resistance.

L27 ANSWER 5 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:467950 HCAPLUS

DN 135:69706
TI Procedure for the production of a **ferroelectric capacitor**.
IN Schindler, Guenther; Hartner, Walter
PA Infineon Technologies A.-G., Germany
SO Ger. Offen., 6 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 19957122	A1	20010628	DE 1999-19957122	19991126

AB With a procedure for manufg. a **ferroelec. capacitor** on a semiconductor substrate a 1st **electrode** of the capacitor is first produced. A **ferroelec. capacitor** material is deposited over the 1st **electrode**. A 2nd **electrode** is produced on the **ferroelec. capacitor** material. Subsequently, the capacitor is subjected to a a.c. treatment, thereby reducing the leakage current in the capacitor by more than a factor 10. A post-annealing process might consequently not be necessary, or can be performed at lower temps. than normally used.
RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 6 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:258975 HCAPLUS
DN 134:374330
TI Studies of ferroelectric film growth and capacitor interface processes via in situ analytical techniques and correlation with electrical properties
AU Krauss, Alan R.; Auciello, Orlando; Dhote, Anil M.; Im, Jaemo; Aggarwal, Sanjeev; Ramesh, Ramamoorthy; Irene, Eugene A.; Gao, Ying; Mueller, Alex H.
CS Materials Science and Chemistry Divisions, Argonne National Laboratory, Argonne, IL, 60439, USA
SO Integrated Ferroelectrics (2001), 32(1-4), 121-131
CODEN: IFEREU; ISSN: 1058-4587
PB Gordon & Breach Science Publishers
DT Journal; General Review
LA English
AB Precise control of compn. and microstructure of multicomponent oxide thin films is crit. for the prodn. of ferroelec. and high dielec. const. thin film devices. In addn., the integration of film-based capacitors with semiconductor substrates for device fabrication requires good control of the compn. and structure of the dielec./substrate and top **electrode**/dielec. interfaces to control the capacitor properties. In order to understand the processes described above, the authors use a variety of integrated complementary in-situ anal. techniques including time-of-flight ion scattering and recoil spectroscopy, XPS, spectroscopic ellipsometry, and ex-situ methods such as TEM microscopy, scanning force microscopy, and SEM. Examples of studies recently performed by their group that are reviewed here include: (1) effects of microstructure on the oxidn. of **Ti-Al** layers that can be used in a dual functionality as a diffusion barrier and bottom **electrode** for integration of **ferroelec. capacitors** with semiconductors; (2) studies of the surface and dielec. layer/bottom **electrode** interface during growth of BaxSr1-xTiO3 films on Ir/**TiN**/SiO2/Si for fabrication of BST capacitors for DRAMs; and (3)

studies of the effect of interface contamination and structure on the elec. properties of BST capacitors for high-frequency devices. 9 Refs.
RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 7 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:73587 HCAPLUS
DN 134:140553
TI Microelectronic devices including **ferroelectric capacitors** with lower **electrodes** extending into contact holes
IN Hwang, Cheol-Seong; Lee, Byoung-Taek
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6180970	B1	20010130	US 1997-909923	19970812
PRAI KR 1996-64012	A	19961210		

AB A microelectronic device includes an insulating layer on a microelectronic substrate in which the insulating layer has a contact hole therein exposing a portion of the microelectronic substrate. A 1st capacitor **electrode** is provided on a surface of the insulating layer opposite the microelectronic substrate and adjacent the contact hole in which a lower portion of the 1st capacitor **electrode** extends into the contact hole below the surface of the insulating layer. A ferroelec. layer is provided on the 1st capacitor **electrode**, and a 2nd capacitor **electrode** is provided on the ferroelec. layer. Related methods and memory devices are also discussed.
RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 8 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:43470 HCAPLUS
DN 134:109248
TI Fabrication of **ferroelec. capacitor** stack for use with an integrated circuit transistor in a ferroelec. memory cell
IN Evans, Thomas A.
PA Ramtron International Corporation, USA
SO U.S., 26 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6174735	B1	20010116	US 1998-177392	19981023
US 6358755	B1	20020319	US 2000-641091	20000817
PRAI US 1998-177392	A3	19981023		

AB A **ferroelec. capacitor** stack for use with an integrated circuit transistor in a ferroelec. memory cell is fabricated. A first dielec. layer is formed over the integrated circuit transistor. A bottom **electrode** is formed over the first dielec. layer, and the bottom **electrode** has a hole located over a first source/drain of the integrated circuit transistor. Over the first dielec. layer and

bottom **electrode** is formed a second dielec. layer, in which a hole is formed to provide access to the bottom **electrode**. A ferroelec. plug is formed in the hole, and a top **electrode** is formed over the second dielec. layer and ferroelec. plug. A third dielec. layer is formed over the second dielec. layer and top **electrode**. A first via is formed through the first, second, and third dielec. layers, and through the hole in the bottom **electrode**. The via has sufficient width to provide access to a lateral edge of the bottom **electrode** hole. A second via is formed through the first, second, and third dielec. layers to provide access to a second transistor source/drain. A third via is formed through the third dielec. layer to provide access to the top **electrode**. The first via, the second via; and the third via are metalized.

RE.CNT 42 THERE ARE 42 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 9 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:900373 HCAPLUS
DN 134:50184
TI Capacitor with ferroelectric or high dielectric constant film and method of fabricating the same
IN Noma, Atsushi; Nakao, Keisaku; Uemoto, Yasuhiro
PA Matsushita Electronics Corporation, Japan
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1061582	A2	20001220	EP 2000-112600	20000614
	EP 1061582	A3	20020619		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	TW 454331	B	20010911	TW 2000-89110090	20000525
	CN 1278108	A	20001227	CN 2000-109004	20000601
	JP 2001060670	A2	20010306	JP 2000-172183	20000608
PRAI	JP 1999-169262	A	19990616		

AB A protective insulating film is deposited on a field-effect transistor formed on a semiconductor substrate. A contact plug having a lower end portion connected to an impurity diffusion layer of the field-effect transistor is formed in the protective insulating film. A conductive diffusion preventing film connected to an upper end portion of the contact plug is formed on the protective insulating film. A capacitor lower **electrode** is formed on the diffusion preventing film. Sidewalls made of an oxidn. resistant material are formed on at least the side surfaces of the diffusion preventing film. A capacitor insulating film made of an insulating metal oxide is formed over the capacitor lower **electrode** and the sidewalls. A capacitor upper **electrode** is formed on the capacitor insulating film.

L27 ANSWER 10 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:592955 HCAPLUS
DN 133:171112
TI Microelectronic device for storing information based on oxides and semiconductors
IN Beck, Armin; Bednorz, Johannes G.; Gerber, Christoph; Rossel, Christophe P.

PA International Business Machines Corporation, USA
SO PCT Int. Appl., 39 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2000049659	A1	20000824	WO 2000-IB43	20000117
W: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
EP 1153434	A1	20011114	EP 2000-900098	20000117
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
PRAI WO 1999-IB283	W	19990217		
WO 2000-IB43	W	20000117		

AB The basic discovery underlying the present invention concerns a plurality of oxide substances, i.e., materials for use in microelectronic and in electronic circuits and particularly semiconductor chips which combine both a switching phenomenon in resistance and a built-in memory. One preferred member of that plurality is BaxSr1-xTiO3 with x = 0-0.7 and having a dopant of Cr between 0% and 5 %, preferably between 0% and 1 %, even more preferably .apprx.0.2%. When said substance was used for example as a dielec. layer in a capacitor-like structure it stays switched in either a high or a low cond. state depending on the voltage pulse being applied to it. Thus it is possible to store digital information by different values of resistance, i.e., by assocg. a high resistance state with a logic 0 and a low resistance state with a logic 1. Such stored information can be read out by measuring the leakage current. Even multi-level switching is realizable.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 11 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:489124 HCAPLUS
DN 133:82870
TI Method for fabricating a high dielectric **ferroelectric capacitor**
IN Kim, Wan-Don; Lee, Byoung-Taek
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6090704	A	20000718	US 1998-113142	19980710
PRAI KR 1997-33350	A	19970716		

AB A method for fabricating a semiconductor device using a high dielec. material as a dielec. film of a capacitor wherein an etch stopping layer

such as BST having a good dry etch selectivity with respect to an interlayer insulating film is formed on the adhesion layer formed on an upper **electrode**. This etch stopping layer prevents the upper **electrode** of a capacitor from being exposed to be etched during forming a metal contact.

L27 ANSWER 12 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:482173 HCAPLUS
DN 133:215991
TI Low temperature (Ba, Sr)TiO3 capacitor process integration (LTB) technology for gigabit scaled DRAMs
AU Hieda, K.; Eguchi, K.; Nakahira, J.; Kiyotoshi, M.; Nakabayashi, M.; Tomita, H.; Izuha, M.; Aoyama, T.; Niwa, S.; Tsunoda, K.; Yamazaki, S.; Lin, J.; Shimada, A.; Nakamura, K.; Kubota, T.; Asano, M.; Hosaka, K.; Fukuzumi, Y.; Ishibashi, Y.; Kohyama, Y.
CS Microelectronics Engineering Laboratory, Toshiba Corporation, Yokohama, 235-8522, Japan
SO Technical Digest - International Electron Devices Meeting (1999) 789-792
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB Low temp. (600.degree.C) (Ba, Sr)TiO3 (BST) capacitor process integration (LTB) based on SrRuO3 (SRO) **electrode** is proposed to achieve gigabit scaled and embedded DRAMs. BST crystg. temp. is successfully reduced by SRO, which has the same perovskite structure as BST film. Chem. Mech. Polishing (CMP) and O3 water etching are developed for a storage node (SN) **electrode** and a plate (PL) **electrode** patterning. A new low temp. post anneal method is also proposed in order to reduce oxygen vacancies at a top **electrode**-BST interface.
RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 13 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:441990 HCAPLUS
DN 133:67387
TI Liquid delivery MOCVD process for deposition of high frequency dielectric materials
IN Roeder, Jeffrey F.; Stauf, Gregory T.
PA Advanced Technology Materials, Inc., USA
SO PCT Int. Appl., 63 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000037712	A1	20000629	WO 1999-US29566	19991213
	W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 6277436	B1	20010821	US 1998-216673	19981218
PRAI	US 1998-216673	A	19981218		

US 1997-979684 A2 19971126

AB A liq. delivery MOCVD method for deposition of dielec. materials such as (Ba, Sr)TiO3 and (Zr, Sn)TiO4, in which metal source compds. are dissolved or suspended in solvent and flash vaporized at temps. of from .apprx.100.degree. to .apprx.300.degree. and carried via a carrier gas such as Ar, N, He, NH3 or the like, into a CVD reactor wherein the precursor vapor is mixed with a metal oxide film on the substrate at a temp. of from .apprx.400.degree. to .apprx.1200.degree. at a CVD chamber pressure of from .apprx.0.1 torr to .apprx.760 torr. The process is carried out in a CVD system contg. a liq. delivery and flash vaporization assembly where the precursors are provided in lines and supplied to vaporize a unit. Such process may for example be employed to form a (Ba, Sr)TiO3 dielec. material wherein at least 60 at.% of the total metal content of the oxide is **Ti**. The high dielec. material of the invention may be used to form capacitive microelectronic device structures for applications such as dynamic random access memories and high frequency capacitors.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 14 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:368781 HCAPLUS
DN 132:355769
TI Chemical mechanical polishing of FERAM capacitors
IN Van Buskirk, Peter C.; Russell, Michael W.; Bilodeau, Steven M.; Baum, Thomas H.
PA Advanced Technology Materials, Inc., USA
SO PCT Int. Appl., 71 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000031794	A1	20000602	WO 1999-US27754	19991123
	W: JP, KR				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6346741	B1	20020212	US 1998-200499	19981125
	EP 1133792	A1	20010919	EP 1999-962839	19991123
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, FI				
PRAI	US 1998-200499	A	19981125		
	US 1997-975366	A2	19971120		
	WO 1999-US27754	W	19991123		

AB A method is claimed of forming a microelectronic device structure, e.g., a **ferroelec. capacitor** structure, using chem. mech. polishing (CMP) for planarizing device layers. The layers may include a barrier layer (28), a bottom **electrode** (30), a ferroelec. layer (32), a top **electrode** (34), and a dielec. insulating layer (35). The barrier layer (28) may serve as a stop layer at the planarization depth in the dielec. insulating material. An insulating layer (38) may be deposited over the structure. The CMP process may include: (I) CMP medium contg. components conferring beneficial properties, (II) metal and dielec. materials to be removed, (III) phys. damage to microelec. device structure being removed by thermal annealing, and (IV) noble metal **electrode** being removed in the planarization by the CMP medium. The microelectronic device structure formed by the CMP may also include conductive lines

embedded in a high magnetic permeability material.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 15 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:259075 HCAPLUS
DN 132:287554
TI Stacked capacitor memory cell devices for DRAMs and fabrication thereof
IN Shen, Hua; Kunkel, Gerhard; Gutsche, Martin
PA Siemens A.-G., Germany
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000114475	A2	20000421	JP 1999-275314	19990928
	US 6136660	A	20001024	US 1998-161861	19980928
	CN 1290038	A	20010404	CN 1999-120763	19990928
PRAI	US 1998-161861	A	19980928		

AB The title capacitors comprise a conductor plug connecting a 1st region, a conductor layer forming a diffusion barrier on the plug, dielec. layer covering over the plug on the barrier layer, a 1st metal layer for an internal **electrode** in the capacitor connected to the barrier layer on the dielec. layer sidewall, a dielec. layer for capacitor dielec. formed over and sidewall of the dielec. layer, and a 2nd metal layer as the capacitor external **electrode** formed over the dielec. layer. The fabrication provides the FETs with compact memory capacitors.

L27 ANSWER 16 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:64096 HCAPLUS
DN 132:201533
TI Plasma etching and electrical characterization of Ir/IrO2/PZT/Ir FeRAM device structures
AU Celii, F. G.; Moise, T. S.; Summerfelt, S. R.; Archer, L.; Chen, P.; Gilbert, S.; Beavers, R.; Bilodeau, S. M.; Vestyck, D. J.; Johnston, S. T.; Russell, M. W.; Van Buskirk, P. C.
CS Texas Instruments, Inc., Dallas, TX, 75265, USA
SO Integrated Ferroelectrics (1999), 27(1-4), 1271-1285
CODEN: IFEREU; ISSN: 1058-4587
PB Gordon & Breach Science Publishers
DT Journal
LA English
AB We report the effect of top **electrode** structure on the elec. properties of ferroelec. Pb(ZrxTi1-x)O3 (PZT) capacitors. Samples with Ir/PZT/Ir or Ir/IrO2/PZT/Ir stacks were prepd. using reactively sputtered Ir/IrO2 (top) and Ir (bottom) **electrodes** and MOCVD-deposited PZT on TiAlN/SiO2/Si wafers. Capacitor structures were patterned by plasma etching of the top **electrode** and show evidence for transient fence formation. Elec. measurements of the capacitors showed good ferroelec. properties (2Pr up to 38 .mu.C/cm2, with leakage <10-6 A/cm2) and low fatigue (<20% drop in Qsw) out to 8.times.1010 cycles. Samples with top **electrode** structures contg. IrO2 gave higher 2Pr values and lower pre-anneal fatigue, when compared with Ir-only top **electrode** samples. The sample with top **electrode** contg. the thinnest IrO2 layer showed slightly lower fatigue than the rest. We also briefly describe the use of these structures and etch methods in

fabricating backend-integrated **ferroelec. capacitors**.
RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L27 ANSWER 17 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:811590 HCAPLUS
DN 132:43722
TI Production of a ferroelectric memory element.
IN Jung, Dong-Jin; Kim, Ki-Nam
PA Samsung Electronics Co. Ltd., S. Korea
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19926711	A1	19991223	DE 1999-19926711	19990611
	KR 2000002485	A	20000115	KR 1998-23272	19980620
	GB 2338595	A1	19991222	GB 1999-9488	19990423
	GB 2338595	B2	20000823		
	TW 418523	B	20010111	TW 1999-88106497	19990423
	CN 1239828	A	19991229	CN 1999-109089	19990618
	US 6172386	B1	20010109	US 1999-335699	19990618
	JP 2000031404	A2	20000128	JP 1999-174714	19990621
PRAI	KR 1998-23272	A	19980620		

AB A **ferroelec. capacitor** with a ferroelec. layer with a comparatively larger **titanium** content than zirconium to improve the ferroelec. properties, is described. The prodn. method of the **ferroelec. capacitor** involves a heat treatment step in an oxygen atm. after the formation of a contact hole in the insulating layer that already covers the formed **ferroelec. capacitor**. Such a heat treatment in an oxygen atm. can minimize the undesired secondary effects of the platinum **electrode** that is known to oxidize the components of the ferroelec. layer.

L27 ANSWER 18 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:659164 HCAPLUS
DN 131:265887
TI Ferroelectric memory device with improved **ferroelectric capacitor** characteristics
IN Shinohara, Sota; Amanuma, Kazushi; Murao, Yukinobu; Katoh, Yuukoh; Takeuchi, Tsuneo; Hayasi, Yoshihiro
PA NEC Corporation, Japan
SO Eur. Pat. Appl., 27 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 949682	A2	19991013	EP 1999-302745	19990408
	EP 949682	A3	19991215		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 11297942	A2	19991029	JP 1998-95846	19980408
	US 6281536	B1	20010828	US 1999-287413	19990407
	CN 1232294	A	19991020	CN 1999-105008	19990408

PRAI JP 1998-95846 A 19980408
AB A ferroelec. memory consists of a **ferroelec. capacitor** formed by depositing a ferroelec. film on a semiconductor substrate. The capacitor includes a lower **electrode** with a ferroelec. film and an upper **electrode**. The upper **electrode** is a laminate of an oxide conductive film of the metal of the **electrode**.

L27 ANSWER 19 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:233720 HCAPLUS
DN 130:305154
TI Manufacture of trench capacitors for memory devices
IN Maijima, Yukihiko
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 11097647	A2	19990409	JP 1997-258593	19970924
JP 3111940	B2	20001127		

AB 1St nitride films of Si, **Al** or **Ti** are formed in the trenches formed in the interlayer insulator films on semiconductor substrates, bottom **electrodes** and dielec. films are buried in the trenches, and 2nd nitride films of Si, **Al** or **Ti** are formed on dielec. films. Capacitors do not deteriorate due to exposure to reductive atm. after their fabrication.

L27 ANSWER 20 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:813645 HCAPLUS
DN 130:89225
TI VLSI semiconductor devices having dielectric or **ferroelectric capacitors** and fabrication thereof
IN Okudaira, Tomohito
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10335581	A2	19981218	JP 1997-140190	19970529

AB The title devices comprise a silica insulative film which holds (1) a peripheral circuit and (2) a capacitor contg. a high-dielec. or ferroelec. insulator bound between upper and lower **electrodes**, wherein contact holes are provided through the silica insulative film to the peripheral circuit and the capacitor. The depth of the contact holes is shorter to the capacitor than to the circuit. The capacitor has a protective high-dielec. or ferroelec. layer provided between the capacitor upper **electrode** and the silica insulative film which covers over the capacitor. The use of the protective dielec./ferroelec. film makes completion of those two contact holes possible at a nearly simultaneously in prevention of plasma damage to the upper **electrode** as well as to the protective barrier metal layer above the **electrode**.

L27 ANSWER 21 OF 31 HCAPLUS COPYRIGHT 2002 ACS

AN 1998:493755 HCAPLUS
DN 129:116725
TI Semiconductor storage device having **ferroelectric capacitor**
IN Miki, Hiroshi; Nakai, Hiromi; Kushida, Keiko; Shimamoto, Yasuhiro; Takatani, Shinichiro; Fujisaki, Yoshihisa
PA Hitachi, Ltd., Japan; Miki, Hiroshi; Nakai, Hiromi; Kushida, Keiko; Shimamoto, Yasuhiro; Takatani, Shinichiro; Fujisaki, Yoshihisa
SO PCT Int. Appl., 57 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9831053	A1	19980716	WO 1998-JP27	19980108
	W: CN, JP, KR, SG, US				
	RW: AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6342712	B1	20020129	US 1999-341523	19990813
	US 2002056862	A1	20020516	US 2001-26615	20011227
PRAI	JP 1997-3571	A	19970113		
	WO 1998-JP27	W	19980108		
	US 1999-341523	A1	19990813		

AB The upper **electrode** of a capacitor is constituted of laminated films which resp. act as a Schottky barrier layer, a hydrogen diffusion preventing layer, a reaction preventing layer, and an adsorption inhibiting layer. Therefore, the occurrence of a capacitance drop, imperfect insulation, and **electrode** peeling in the semiconductor device due to a reducing atm. can be prevented. In addn., the long-term reliability of the device can be improved.

L27 ANSWER 22 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:328398 HCAPLUS
DN 129:88732
TI Microstructure investigations and structure-property correlations in ferroelectric thin film capacitors
AU Li, H.; Yang, B.; Dhote, A.; Aggarwal, S.; Salamanca-Riba, L.; Ramesh, R.
CS Dept. of Materials & Nuclear Eng., Uni. of Maryland, College Park, MD, 20742, USA
SO Materials Research Society Symposium Proceedings (1998), 493(Ferroelectric Thin Films VI), 171-176
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal
LA English
AB Epitaxial 0%, 3% and 10% La doped PZT capacitors with a LSCO bottom **electrode** grown by pulsed laser deposition on Si using a **Ti(Al)N**/Pt conducting barrier layer were systematically studied. **Ferroelec. capacitors** substituted with 10% La show a significantly lower coercive voltage compared to capacitors with 0% and 3% La. This is attributed to the systematic variation of the domain structure of the PLZT film with the increase of La concn. The in-plane orientation relationship of this heterostructure is: [110]PLZT//[110]LSCO//[110]Pt//[110]**Ti(Al)N**//[110]Si. The morphol. of the domains as a function of La concn. was studied using high resoln. transmission electron microscopy(HREM). The Pt/**Ti(Al)N** conducting barrier layer stack is intact after the deposition of the LSCO/PLZT/LSCO stack. All **Ti(Al)N** layers in

the samples studied consist of column-like structures with a [110] texture.

L27 ANSWER 23 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:260440 HCAPLUS
DN 129:11540
TI The effect of **Al**/Pt interface reaction on lead-zirconate-titanate capacitor and the optimization of via contact for double metal ferroelectric RAM
AU Hwang, Yoo-Sang; Lee, Jin-Woo; Lee, Sung-Yung; Koo, Bon-Jae; Jung, Dong-Jin; Chun, Yoon-Soo; Lee, Mi-Hyang; Shin, Dong-Won; Shin, Soo-Ho; Lee, Sang-Eun; Kim, Byung-Hee; Kang, Nam-Soo; Kim, Ki-Nam
CS Technology Development, Semiconductor R&D Center, Samsung Electronics Co., Kyungki-Do, S. Korea
SO Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (1998), 37(3B), 1332-1335
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB The effect of the platinum and **aluminum** interface reaction on the capacitor properties were studied in 64k ferroelec. random access memory (RAM). **Aluminum** diffused into platinum and reacted to form an intermetallic compd. during the post-anneal when **aluminum** had direct contact with the top platinum layer of the **ferroelec**. **capacitor**. The **Al**/Pt/PZT contact was changed into an **Al**-Pt and lead-zirconate-titanate contact by the reaction. As a result, ferroelec. properties degraded and the leakage current of the top **electrode** and lead-zirconate-titanate contact started to increase after annealing at 300.degree.. The capacitor structure was destroyed by the vol. expansion due to the **Al**/Pt reaction at 400.degree.. To prevent this reaction, a **TiN** layer was introduced as the barrier layer. This contact scheme showed no breakdown of the **ferroelec** . **capacitor** up to 400.degree., which indicated that **TiN** acts as a good diffusion barrier for the double-metal process.

L27 ANSWER 24 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:238652 HCAPLUS
DN 128:302836
TI Epitaxial BSTO **ferroelectric capacitor** for giga-bit memory applications
AU Kawakubo, T.; Abe, K.; Sano, K.; Yanase, N.
CS Materials and Devices Research Labs., RandD Center, TOSHIBA Corporation, Kawasaki, 210, Japan
SO Report of Research Center of Ion Beam Technology, Hosei University, Supplement (1998), 16, 11-16
CODEN: RCISDS; ISSN: 0914-2908
PB Hosei Daigaku Ion Bimu Kogaku Kenkyusho
DT Journal
LA English
AB **Ferroelec**. **capacitor** cells were fabricated using a (Ba,Sr)TiO3/SrRuO3 heteroepitaxial technique on strontium titanate and Si substrates. Distinct ferroelectricity results from the c-axis being elongated due to lattice mismatch between the dielec. and **electrode**. The epitaxial BSTO capacitor showed ferroelectricity even at 30 nm thickness. An integration process to obtain an epitaxial capacitor was also developed using Si substrates. An epitaxial (**Ti**,**Al**)N barrier metal showed excellent oxidization

resistance, and prevented Si oxidization during oxide **electrode** and dielec. film formation. Superior ferroelec. properties, reliability, and sub-micron silicon process compatibility of the epitaxial BSTO capacitor were confirmed.

L27 ANSWER 25 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:70954 HCAPLUS
DN 128:109550
TI Semiconductor memory device and its fabrication method.
IN Miki, Hiroshi; Fujisaki, Yoshihisa; Fukuda, Takuya; Kobayashi, Nobuyoshi
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 10022470	A2	19980123	JP 1996-172022	19960702

AB A high-speed semiconductor memory device comprises an org. ferroelec. material such as poly(vinylidene fluoride) or trifluoroethylene-vinylidene fluoride copolymer for the dielec. layer of a memory capacitor. Addnl., the poly(vinylidene fluoride) may contain Pb titanate or Pb titanate zirconate, and the dielec. layer may be formed on the capacitor **electrode** such as **Al**, W, or **TiN** via a barrier layer such as a Si oxide or nitride film. A method for fabricating the device is also described.

L27 ANSWER 26 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:770647 HCAPLUS
DN 128:109115
TI Low voltage performance of Pb(Zr,**Ti**)O3 capacitors through donor doping
AU Yang, B.; Song, T. K.; Aggarwal, S.; Ramesh, R.
CS University of Maryland, and Center for Superconductivity Research, Department of Materials + Nuclear Engineering, College Park, MD, 20742, USA
SO Applied Physics Letters (1997), 71(24), 3578-3580
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB We report low voltage (1.5-3 V) performance of ferroelec. Pb(Zr,**Ti**)O3 based capacitors. La substitution up to 10 was performed to systematically lower the coercive and satn. voltages of epitaxial **ferroelec. capacitors** grown on Si using a (Ti0.9Al0.1)N/Pt conducting barrier composite. **Ferroelec. capacitors** substituted with 10 La show significantly lower coercive voltage compared to capacitors with 0% and 3% La. This is attributed to a systematic decrease in the tetragonality (i.e., c/a ratio) of the ferroelec. phase. Furthermore, the samples doped with 10% La showed dramatically better retention and pulse width dependent polarization compared to the capacitors with 0% and 3% La. These capacitors show promise as storage elements in low power high d. memory architectures.

L27 ANSWER 27 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:716612 HCAPLUS

DN 128:42389
TI Novel ferroelectric epitaxial (Ba,Sr)TiO3 capacitor for deep sub-micron memory applications
AU Kawakubo, T.; Abe, K.; Komatsu, S.; Sano, K.; Yanase, N.; Mochizuki, H.
CS Mater. and Devices Res. Labs., R&D Cent., Toshiba Corp., Kawasaki, 210, Japan
SO IEEE Electron Device Letters (1997), 18(11), 529-531
CODEN: EDLEDZ; ISSN: 0741-3106
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
AB A novel **ferroelec. capacitor** cell was developed using a (Ba,Sr)TiO3 (BSTO)/SrRuO3 (SRO) heteroepitaxial technique on Si and strontium titanate substrates. Distinct ferroelectricity results from the c-axis being elongated due to lattice mismatch between the dielec. and **electrode**. The epitaxial BSTO capacitor showed distinct ferroelectricity even at 30 nm thickness, which is the thinnest ferroelec. film so far. Its superior ferroelec. properties, reliability, and sub-micron silicon process compatibility were confirmed.

L27 ANSWER 28 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:424667 HCAPLUS
DN 127:59155
TI Semiconductor apparatus having ferroelectric thin film capacitor
IN Kuroda, Yoshiki
PA Olympus Optical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09116111	A2	19970502	JP 1995-274197	19951023

AB In the capacitor, the upper- and/or lower **electrode** comprise a first **electrode** which is unreactive at a temp. of the ferroelec. film heat treatment, and a second **electrode** contg. a metal (or an alloy) with sp. resistivity 1.0-3.0 .mu..OMEGA.-cm. Heating may be applied in manuf. of the capacitor using a heat-resistant **electrode**.

L27 ANSWER 29 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:569536 HCAPLUS
DN 125:210324
TI Semiconductor nonvolatile memory device and manufacture thereof
IN Naiki, Tadaya
PA Sony Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08172168	A2	19960702	JP 1994-334848	19941220

AB A semiconductor nonvolatile memory device, consisting of an array of **ferroelec. capacitor** memory cells, wherein the lower **electrode** conductor layer serves also as the memory cell circuit.

L27 ANSWER 30 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:810454 HCAPLUS
DN 123:215917
TI Ferroelectric memory devices
IN Watanabe, Hitoshi; Kuroda, Yoshiki; Tadokoro, Kaoru
PA Olympus Optical Co., Ltd., Japan; Symetrix Corp.
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07111318	A2	19950425	JP 1993-254378	19931012

AB The device has a **ferroelec. capacitor** which consists of a lower **electrode**, an oxide ferroelec. film, and an upper **electrode** sequentially formed on a semiconductor substrate, and a protective film contg. a nitride of **Al**, Si, or **Ti** as a main component on the capacitor. The protective film may have the compn. same with that or component(s) common to those of the oxide ferroelec. film. The ferroelec. oxide film may consist of a Bi-layered perovskite-type compd. of (Bi2O2)2+(Am-1BmO3m+1)2- (A = Bi, Pb, Ba, Sr, Ca, Na, K, and/or Cd; B = **Ti**, Nb, Ta, W, Mo, Fe, Co, and/or Cr); m = 1-5 (integer) having concn. of B graded in the thickness direction and concd. at the interface with the upper **electrode**. Redn. and alteration of the oxide ferroelec. film at its surfaces are prevented, and peeling of the **electrodes** off the oxide ferroelec. film is suppressed.

L27 ANSWER 31 OF 31 HCAPLUS COPYRIGHT 2002 ACS
AN 1992:624464 HCAPLUS
DN 117:224464
TI Semiconductor devices containing transistors and capacitors
IN Takenaka, Kazuhiro
PA Seiko Epson Corp., Japan
SO PCT Int. Appl., 33 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9206498	A1	19920416	WO 1991-JP1280	19910926
	W: JP, KR, US				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LU, NL, SE				
	EP 503078	A1	19920916	EP 1991-916783	19910926
	EP 503078	B1	20010606		
	R: DE, FR, GB, IT, NL				
	JP 2001111001	A2	20010420	JP 2000-275535	19910926
	JP 3185220	B2	20010709	JP 1991-515297	19910926
	US 5475248	A	19951212	US 1994-303134	19940908
PRAI	JP 1990-259455	A	19900928		
	JP 1991-515297	A3	19910926		
	WO 1991-JP1280	W	19910926		
	US 1992-867238	B1	19920716		
	US 1993-166796	B1	19931213		

AB A semiconductor device (e.g., erasable and programmable ROM) contains a

transistor comprising a gate **electrode**, and source and drain regions, as well as a **ferroelec**. **capacitor** on a local oxide film. The capacitor has a ferroelec. film sandwiched between upper and lower **electrodes**. The upper **electrode** and the source region are connected by a wiring in which a conductive film for preventing reactions and a wiring **electrode** comprising **Al** are deposited. The conductive film may be formed of **TiN**, MoSi, or W. Even when, after forming the wiring **electrode**, an annealing treatment is performed or a final protective film is formed for improving characteristics, the wiring **electrode** does not react with the upper **electrode**, and a good ferroelec. film characteristic is obtained.

L32 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:315426 HCAPLUS
DN 136:333966
TI Method of patterning noble metals for semiconductor devices by electropolishing
IN Lane, Richard H.
PA USA
SO U.S. Pat. Appl. Publ., 15 pp., Division of U.S. Ser. No. 639,089.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002048870	A1	20020425	US 2001-989372	20011121
PRAI	US 2000-639089	A3	20000816		

AB An electropolishing process for high resoln. patterning of noble metals, such as Pt, for forming various semiconductor devices, such as capacitors or wiring patterns is disclosed.

L32 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:537479 HCAPLUS
DN 135:100895
TI Iridium and platinum etching methods for anisotropic profile production of contacts in integrated circuits
IN Hwang, Jeng H.; Ying, Chentsau; Jin, Guang Xiang; Mak, Steve S. Y.
PA Applied Materials, Inc., USA
SO U.S., 47 pp., Cont.-in-part of U.S. Ser. No. 6,092.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6265318	B1	20010724	US 1999-251633	19990217
	WO 2000049650	A1	20000824	WO 2000-US4058	20000216
	W: JP, KR				
	WO 2000049651	A1	20000824	WO 2000-US4240	20000217
	W: JP, KR				
PRAI	US 1998-6092	A2	19980113		
	US 1999-251588	A	19990217		
	US 1999-251633	A	19990217		
	US 1999-251826	A	19990217		
	US 1999-421467	A	19991019		

AB A method of etching an **electrode** layer (e.g., a Pt **electrode** layer or an Ir **electrode** layer) disposed on a substrate to produce a semiconductor device including a plurality of **electrodes** sepd. by a distance equal to or .ltorsim.0.3 .mu.m and having a profile equal to or .gtorsim.85.degree.. The method comprises heating the substrate to a temp. .gtorsim.150.degree.., and etching the **electrode** layer by employing a high d. inductively coupled plasma of an etchant gas comprising O and/or Cl, Ar and a gas selected from the group consisting of BCl3, HBr, HCl and mixts. thereof. A semiconductor device having a substrate and a plurality of **electrodes** supported by the substrate. The **electrodes** have a dimension (e.g., a width) which include a value equal to or .ltorsim.0.3 .mu.m and a profile equal to or .gtorsim.85.degree..

RE.CNT 54 THERE ARE 54 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 3 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:449935 HCAPLUS
DN 135:39677
TI Hydrogen barrier encapsulation techniques for the control of hydrogen induced degradation of **ferroelectric capacitors** in conjunction with multilevel metal processing for non-volatile integrated circuit memory devices
IN Bailey, Richard A.
PA Ramtron International Corporation, USA
SO U.S., 24 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6249014	B1	20010619	US 1998-164952	19981001

AB A H barrier encapsulation technique for the control of H induced degrdn. of **ferroelec. capacitors** in nonvolatile integrated circuit memory devices. The resultant device structure ameliorates the H induced degrdn. of **ferroelec. capacitors** by completely encapsulating the capacitor within a suitable H barrier material, such as CVD (CVD) or sputtered Si nitride, thus ensuring process compatibility with industry std. process steps. Although the deposition process for CVD Si3N4 itself contains H, the deposition time may be kept relatively short thereby allowing the **TiN** local interconnect layer to act as a short term H barrier. The techniques of the present invention are applicable to all known ferroelec. dielecs. including perovskites and layered perovskites (whether doped or undoped) including PZT, PLZT, BST, SBT and others while simultaneously allowing for a potentially broader choice of **electrode** materials and the use of a forming gas anneal process step on the completed IC structure.
RE.CNT 33 THERE ARE 33 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:394073 HCAPLUS
DN 135:13054
TI Non volatile ferro-electrical memory and procedure for its production.
IN Kang, Hee Bok
PA Hyundai Electronics Industries Co., Ltd., Ichon, S. Korea
SO Ger. Offen., 62 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
DE 10054595	A1	20010531	DE 2000-10054595	20001103
JP 2001156265	A2	20010608	JP 2000-340188	20001108
PRAI KR 1999-51975	A	19991122		

AB A non-volatile ferroelec. memory and a procedure for its prodn. are described. The non-volatile ferroelec. memory is provided with the following: a no. of 1st gate **electrodes** and 2nd gate **electrodes**, which are elec. sep. from each other and are formed on

an active area of a substrate: a no. of 1st **electrodes** of 1st **ferroelec. capacitors**, which are connected with the substrate on a side of the 1st gate **electrode**, and a no. of 1st **electrodes** of 2nd **ferroelec. capacitors**, which are connected with the substrate on a side of the 2nd gate **electrode** in each case; ferroelec. layers, which are formed on the 1st **electrodes** in each case; 2nd **electrodes** of the 1st **ferroelec. capacitors** and 2nd **electrodes** of the 2nd **ferroelec. capacitors**, which are formed on resp. ferroelec. layers; and a 1st metal line, connecting the no. 1st gate **electrodes** elec., and a 2nd metal line connecting the no. of 2nd gate **electrodes** elec. The manuf. process is simplified and the memory capacity is increased using this procedure and lastly the packing d. is increased without increasing the capacitor surface area.

L32 ANSWER 5 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:508178 HCAPLUS
DN 133:98154
TI Method of fabricating a contact structure having a composite barrier layer between a platinum layer and a polysilicon plug
IN Schuele, Paul J.; Fazan, Pierre C.
PA Micron Technology, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6093615	A	20000725	US 1994-290655	19940815
	US 6313031	B1	20011106	US 2000-535050	20000324
	US 2002004299	A1	20020110	US 2001-944436	20010831
PRAI	US 1994-290655	A1	19940815		
	US 2000-535050	A1	20000324		

AB This invention is a process for forming an effective Ti nitride barrier layer between the upper surface of a polysilicon plug formed in thick dielec. layer and a Pt lower capacitor plate in a dynamic random access memory which is being fabricated on a Si wafer. The barrier layer process begins by etching the upper surface of the polysilicon plug using a selective polysilicon etch until it is recessed at least 1000 .ANG. below the upper surface of the thick dielec. layer. Using a collimated sputter source, a Ti layer having a thickness of 100-500 .ANG. is deposited over the surface of the in-process wafer, thus covering the upper surfaces of the polysilicon plugs. A layer of amorphous Ti carbonitride having a thickness of 100-300 .ANG. is then deposited via low-pressure CVD. This is followed by the deposition of a reactively sputtered Ti nitride layer having a thickness of 1000-2000 .ANG.. The wafer is then planarized to remove the Ti, Ti carbonitride and Ti nitride, except that which is in the recesses on top of the Si plugs. The wafer is then annealed in N to react the Ti layer with the Si on the upper surfaces of the plugs to form Ti silicide. A Pt layer is then deposited and patterned to form lower capacitor **electrodes** which are elec. coupled to the polysilicon plugs through the Ti silicide, Ti nitride and Ti carbonitride layers.
RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:461208 HCAPLUS

DN 133:52170
TI Stacked MOS capacitor fabrication for DRAM
IN Huang, Kuo-tai; Hsieh, Wen-yi; Yew, Tri-rung
PA United Microelectronics, Corp., Taiwan
SO Brit. UK Pat. Appl., 25 pp.
CODEN: BAXXDU
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 2340303	A1	20000216	GB 1998-17261	19980807
	GB 2340303	B2	20001227		

AB A contact window is formed in the interlayer dielec. film self-aligned with respect to the gate sidewall spacers which exposes the source/drain region common to the adjacent transistors. A cylindrical capacitor with a metal **electrode** (Ti), a diffusion barrier (**TiN**), a high dielec. const. layer (Ta2O5), and a plate **electrode** (WN, Pt, or RuO2) is formed in the window and extends across the whole common source/drain region. This increases the storage capacity.

L32 ANSWER 7 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:418369 HCAPLUS
DN 131:152234
TI High temperature platinum etching using Ti mask layer
AU Kim, Hyoun-woo; Ju, Byong-Sun; Nam, Byeong-Yun; Yoo, Won-Jong; Kang, Chang-Jin; Ahn, Tae-Hyuk; Moon, Joo-Tae; Lee, Moon-Yong
CS Semiconductor R&D Center, Samsung Electronics, Yongin-City, Kyungki-Do, S. Korea
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (1999), 17(4, Pt. 2), 2151-2155
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB Platinum is a strong candidate for an **electrode** material of **ferroelec. capacitors** in highly integrated dynamic random access memory devices. However, it is extremely difficult to etch fine patterns of Pt owing to an inherently low etch slope. This characteristic comes from the phys. sputtering nature of the Pt etching process. This article reveals that the Pt etching profile depends on the change of the Ti mask layer caused by the increase of wafer temp. during etching. A Pt etching slope of 80.degree. with 0.40 .mu.m pitch was attained by heating the wafer substrate up to 220.degree. in a plasma. From transmission electron microscopic anal. the Ti mask is converted to TiOx in oxygen plasma at high wafer temp., elevated either by high **electrode** temp. or plasma irradn.
RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L32 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:578879 HCAPLUS
DN 129:297027
TI Growth and characterization of radio-frequency magnetron sputtered lead zirconate titanate thin films deposited on .ltbbrac.111.rtbbrac. Pt **electrodes***
AU Ea-Kim, B.; Aubert, P.; Ayguavives, F.; Bisaro, R.; Varniere, F.; Olivier, J.; Puech, M.; Agius, B.

CS BP 127, Universite de Paris Sud, Orsay, 91403, Fr.
SO Journal of Vacuum Science & Technology, A: Vacuum, Surfaces, and Films (1998), 16(5), 2876-2884
CODEN: JVTAD6; ISSN: 0734-2101
PB American Institute of Physics
DT Journal
LA English
AB The phys., chem., and elec. quality of the bottom **electrode** plays a key role in the fabrication of **ferroelec. capacitors**. The authors used x-ray diffraction and TEM to study the stability of the Pt/**TiN**/Ti/SiO2/Si stack before PZT film studies. The Pt layer deposited by radiofrequency (rf) magnetron sputtering on such structure was strongly .ltbbrac.111.rtbbrac. oriented. The nucleation, growth, and orientation of lead zirconate titanate [Pb(Zr0.40Ti0.60)O3] thin film, performed by radiofrequency magnetron sputtering from ceramic target on .ltbbrac.111.rtbbrac. oriented Pt **electrode** and crystd. by rapid thermal annealing, were studied. The studies reveal that the PZT thin films deposited at 200.degree., with a substrate-target distance equal to 5.5 cm, using 1 Pa Ar pressure, and plasma power d. of 1.7 W/cm2 allow good control of the film compn. The optimal annealing conditions were then detd. to achieve a pure perovskite structure (mainly .ltbbrac.111.rtbbrac. oriented). Ferroelec. hysteresis loop measurements indicated a remanent polarization of 22.0 .mu.C/cm2 and coercive field of 50 kV/cm for the phase compn. Zr/Ti = 40/60.

L32 ANSWER 9 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:712142 HCAPLUS
DN 126:97779
TI Fabrication of ferroelectric PZT thin film capacitors with indium **tin** oxide (ITO) **electrodes**
AU Rao, Ashok V.; Mansour, Said A.; Bement, , Arden L. Jr.
CS School of Materials Engineering, Purdue University, West Lafayette, USA
SO Materials Letters (1996), 29(4-6), 255-258
CODEN: MLETDJ; ISSN: 0167-577X
PB Elsevier
DT Journal
LA English
AB Conductive metal oxide contacts were used in the fabrication of fatigue-resistant lead zirconate titanate (PZT) capacitors. The successful fabrication and characterization of PZT thin-film capacitors with transparent conducting In Sn oxide (ITO) contacts using a combination of metallo-org. decompn. (MOD) and radiofrequency-sputtering are described. High remnant polarization, improved fatigue resistance, and a leakage c.d. of 10-4 A/cm2 were found in ITO-PZT-ITO capacitors.

L32 ANSWER 10 OF 10 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:229071 HCAPLUS
DN 124:276180
TI Forming a layered local interconnect compatible with integrated circuit **ferroelectric capacitors**
IN Eastep, Brian
PA Ramtron International Corp., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

PI	US 5498569	A	19960312	US 1994-294077	19940822

AB A method of forming a local interconnect for a ferroelec. memory cell includes the steps of simultaneously opening top **electrode** and source/drain contacts to the ferroelec. memory cell, sputtering a 1st blanket metal layer comprised of Pt or Pd on the top surface of the ferroelec. memory cell, annealing the ferroelec. memory cell to simultaneously recover damage in the **ferroelec**. **capacitor** dielec. of the memory cell, and to silicide the 1st metal layer in the source/drain contact, sputtering a 2nd blanket metal layer comprised of Ti nitride on the top surface of the 1st metal layer, and selectively etching the 1st and 2nd metal layers to form the local interconnect between the top **electrode** and source/drain contacts of the ferroelec. memory cell.

L34 ANSWER 1 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:69696 HCAPLUS
DN 136:111371
TI Capacitor **electrode** using catalytic metal for semiconductor memory device and precursor material for the **electrode**
IN Koike, Toshiyuki; Kurita, Masaaki
PA Tanaka Noble Metal Sales Co., Ltd., Japan; Tanaka Noble Metal Industrial Co., Ltd.
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002025908	A2	20020125	JP 2000-204693	20000706

PI JP 2002025908 A2 20020125 JP 2000-204693 20000706
AB The **electrode**, for the memory device capacitor involving a metal oxide dielec. layer, contains a catalytic metal and a catalyst poison for preventing redn. of the dielec. metal oxide catalyzed by the metal in heating in manuf. of the memory device. The **electrode** precursor contains the catalytic metal and the catalyst poison as their combination, preferably as a sputtering target, or independently, preferably as organometallic compds. for metalorg. **CVD**.

L34 ANSWER 2 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:10930 HCAPLUS
DN 136:78291
TI Method for fabricating semiconductor memory device
IN Choi, Eun-Seok; Yeom, Seung-Jin
PA S. Korea
SO U.S. Pat. Appl. Publ., 5 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002000594	A1	20020103	US 2001-892537	20010628

PI US 2002000594 A1 20020103 US 2001-892537 20010628
PRAI KR 2000-37353 A 20000630
AB A semiconductor memory device is provided which prevents a lifting phenomenon by improving an adhesive strength between an upper **electrode** and an interlayer insulating layer. The semiconductor memory device includes a capacitor formed on a semiconductor substrate, in which the capacitor includes a lower **electrode**, a dielec. layer and an upper **electrode**; an adhesion layer formed on the upper **electrode**; an interlayer insulating layer covering the capacitor, in which a portion of the interlayer insulating layer is in contact with the adhesion layer; and a contact hole, formed within the interlayer insulating layer, whose bottom exposes the upper **electrode** and whose sidewalls expose the interlayer insulating layer and the adhesion layer.

L34 ANSWER 3 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:541487 HCAPLUS
DN 135:101137
TI Procedure for the fabrication of a nonvolatile DRAM memory cell from **ferroelectric capacitor** using tungsten **CVD** as

protective layer
IN Hartner, Walter; Schindler, Guenther; Kastner, Marcus
PA Infineon Technologies A.-G., Germany
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DE 10001118	A1	20010726	DE 2000-10001118	20000113
US 2001018237	A1	20010830	US 2001-761807	20010116
PRAI DE 2000-10001118	A	20000113		

AB During the prodn. of a DRAM memory cell with switching transistor (2) and storage capacitor (3), contg. a ferroelec. dielec. (32) and platinum capacitor **electrodes** (31, 33a), on the upper **electrode** (33a) in the area of contact hole (51) formed in an insulating layer (5) a conductive protective layer (33b) is applied by W **CVD** in H2 atmosphere into the contact hole without the dielec. (32) being reduced by the H under catalytic action of Pt.
RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 4 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:292604 HCAPLUS
DN 135:85250
TI Indium doped **tin** oxide as **electrode** of ferroelectric films
AU Li, Jinhua; Chen, Hansong; Li, Kun; Tang, Guoying; Chen, Wanglihua
CS Functional Materials Lab., Jiangsu Institute of Petrochemical Technology, Changzhou, 213016, Peop. Rep. China
SO Gongneng Cailiao (2001), 32(1), 64-66
CODEN: GOCAEA; ISSN: 1001-9731
PB Gongneng Cailiao Bianjibu
DT Journal
LA Chinese
AB The indium doped **tin** oxide (ITO) films were prepd. by sol-gel precess on SiO2/Si and borosilicate glass substrates with ITO sol and SnO2, and their formation and crystn. were studied by XRD. The results showed that sol-gel ITO films on SiO2/Si and glass substrates had good crystallinity and conduction like ITO formed by **CVD** on borosilicate glass, but sol-gel PLT and PZT films could not form obvious texture on the sol-gel ITO film as bottom **electrode**. The sol-gel ITO films could not be used as top **electrode** for sol-gel PLT and PZT because of the large leakage, but the Au/PLT/ITO (**CVD**) **ferroelec. capacitor** with good elec. properties could be obtained.

L34 ANSWER 5 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:258953 HCAPLUS
DN 135:12848
TI Integration of H2 barriers for ferroelectric memories based on SrBi2Ta2O9 (SBT)
AU Hartner, Walter; Schindler, Gunther; Bosk, Peter; Gabric, Zonimir; Kastner, Markus; Beitel, Gerhard; Mikolajick, Thomas; Dehm, Christine; Mazure, Carlos
CS Infineon Technologies AG, Munich, 81730, Germany
SO Integrated Ferroelectrics (2000), 31(1-4), 273-284

CODEN: IFEREU; ISSN: 1058-4587
PB Gordon & Breach Science Publishers
DT Journal
LA English
AB Integration of an H barrier into a FeRAM process flow was studied. It is reported in the literature that ferroelec. properties can be maintained after H annealing by using IrOx as a top **electrode** [16][17][18]. Advantage of materials like IrOx is less catalytic activity compared to Pt. However, IrOx is not a promising candidate for top **electrode** barrier. (Pt)/IrOx/SBT/Pt capacitors are prone to shorting or exhibit high leakage. IrOx films are very easily reduced by reducing ambient which will result in peeling off. Also, IrOx films tend to oxidize Ti or **TiN** layers immediately. Therefore, other barrier materials or layer sequences like Ir/IrOx have to be considered. For protection of the entire capacitor an Encapsulation Barrier Layer (EBL) is required. **LPCVD** SiN was used. **LPCVD** SiN is a std. material in CMOS technol. Prodn. tools are available and it is known as H barrier. By modifying the deposition process and using a novel process sequence, no visual damage of the capacitors after SiN-deposition and FGA is seen. Also, no degrdn. of elec. properties after capacitor formation as well as after SiN-deposition and FGA is obsd. However, after metal 1 and metal 2 processing, 2Pr values at 1.8 V are reduced from 12.mu.C/cm2to 2.mu.C/cm2. Polarization at 5.0 V is not affected.
RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 6 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:195132 HCAPLUS
DN 134:216122
TI Method for manufacturing **ferroelectric capacitor** with hydrogen diffusion barrier
IN Kim, Young Bog
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6204070	B1	20010320	US 1998-221622	19981228
PRAI KR 1997-75076	A	19971227		

AB The present invention relates to a method for manufg. **ferroelec. capacitor**, capable of preventing the H gas generated in the process for the overlying interlayer insulating layer from being diffused into the underlying ferroelec. material film and/or the 1st diffusion barrier TiO2 film, thereby eliminating the aggravation of the characteristics of the **ferroelec. capacitor**. As ferroelec. material film, SrBi2-xTa2O9-x (simply SBT) film or PZT film can be formed. For PZT film, TiO2 was used for a 1st diffusion barrier film, Si nitride such as Si3N4 or SiON was used for a 2nd diffusion barrier film, and SiO2 film can be provided under the Si nitride film as a stress buffer film. Alternatively, for the SBT, a Si nitride film is provided as a diffusion barrier film and a SiO2 film is further provided under the Si nitride film as a stress buffer film. Such a Si nitride film prevents H or O generated in the following process from being introduced into the underlying ferroelec. material film. Thus, the ferroelec. material can be remain stable in stoichiometry in relatively long time, thereby improve

the reliability thereof.
RE.CNT 15 THERE ARE 15 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 7 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:736204 HCAPLUS
DN 133:304488
TI Amorphously deposited metal oxide ferroelectric ceramic films for capacitor applications
IN Hintermaier, Frank S.; Hendrix, Bryan C.; Roeder, Jeffrey F.; Desrochers, Debra A.; Baum, Thomas H.
PA Advanced Technology Materials, Inc., USA
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6133051	A	20001017	US 1998-107861	19980630
	US 6350643	B1	20020226	US 1998-216370	19981218
PRAI	US 1997-68040P	P	19971218		
	US 1998-107861	A2	19980630		

AB A metal oxide ceramic layer is formed from an amorphous film. The metal oxide ceramic layer comprises, e.g., a Bi-based oxide ceramic. The amorphous Bi-based metal oxide layer is annealed to transformed it into a ferroelec. layer. A lower thermal budget is needed to transform the amorphous Bi-based metal oxide ceramic into the ferroelec. phase.
RE.CNT 34 THERE ARE 34 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 8 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:737484 HCAPLUS
DN 131:358854
TI A novel low-temperature (Ba,Sr)TiO3 (BST) process with Ti/**TiN** barrier for Gbit DRAM applications
AU Beitel, G.; Wendt, H.; Fritsch, E.; Weinrich, V.; Engelhardt, M.; Hasler, B.; Rohr, T.; Bergmann, R.; Scheler, U.; Malek, K.-H.; Nagel, N.; Gschwandtner, A.; Pamler, W.; Honlein, W.; Dehm, C.; Mazure, C.
CS Infineon Technologies AG, Munich, D-81739, Germany
SO Microelectronic Engineering (1999), 48(1-4), 299-302
CODEN: MIENEF; ISSN: 0167-9317
PB Elsevier Science B.V.
DT Journal
LA English
AB A new, low temp. (Ba,Sr)TiO3 (BST) **MOCVD** process has been established at 580.degree. deposition temp. which can be used for Gbit DRAM applications using Ti/**TiN** as barrier material. The process window for BST deposition was studied in terms of deposition temp., stoichiometry, film thickness, post annealing treatment and variation of the underlying **electrode**/barrier layer. Elec. characterization revealed specific capacitance values of 45 fF/.mu.m2 for 25-30 nm film thickness and 75 fF/.mu.m2 for 10 nm film thickness which is close to the target value for Gbit of 80-100 fF/.mu.m2. Oxidn. resistance of the Ti/**TiN** barrier could be shown up to 600.degree.. Feasibility of this low temp. BST process has been successfully demonstrated using a 4 Mbit test vehicle.
RE.CNT 2 THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD

ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 9 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:529076 HCAPLUS
DN 131:137977
TI Fabricating individual, embedded capacitors for laminated printed circuit boards
IN Brandt, Lutz W.; Matijasevic, Goran; Gandhi, Pradeep R.
PA Ormet Corporation, USA
SO PCT Int. Appl., 23 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9941019	A1	19990819	WO 1999-US2790	19990209
	W: CA, JP				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
PRAI	US 1998-21967		19980211		

AB A method of fabricating individual, embedded capacitors in multilayer printed circuit boards is disclosed. The method is compatible with std. printed circuit board fabrication. The capacitor fabrication is based on a sequential build-up technol. employing a 1st patternable insulator. After patterning of the insulator, pattern grooves are filled with a high dielec. const. material, typically a polymer/ceramic composite. Capacitance values are defined by the pattern size, thickness and dielec. const. of the composite. Capacitor **electrodes** and other elec. circuitry can be created either by etching laminated Cu, by metal evapn. or by depositing conductive ink.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 10 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:35023 HCAPLUS
DN 130:118211
TI Low-temperature **chemical vapor deposition** process for forming bismuth-containing ceramic thin films useful in ferroelectric memory devices
IN Hintermaier, Frank S.; Dehm, Christine; Hoenlein, Wolfgang; Van, Buskirk Peter C.; Roeder, Jeffrey F.; Hendrix, Bryan C.; Baum, Thomas H.; Desrochers, Debra A.
PA Advanced Technology Materials, Inc., USA; Siemens Aktiengesellschaft
SO PCT Int. Appl., 53 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9900530	A1	19990107	WO 1998-US13470	19980626
	W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES,				

FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG

US 6303391	B1	20011016	US 1997-975087	19971120
AU 9883774	A1	19990119	AU 1998-83774	19980626
EP 990059	A1	20000405	EP 1998-934193	19980626
R: BE, DE, FR, GB, IT				
JP 2001521584	T2	20011106	JP 1999-505841	19980626
US 2001041374	A1	20011115	US 2001-873138	20010601
PRAI US 1997-50081P	P	19970626		
US 1997-975087	A	19971120		
WO 1998-US13470	W	19980626		

OS MARPAT 130:118211

AB The Bi-contg. film can be formed using a tris(.beta.-diketonate) Bi precursor. Films of amorphous SBT can be formed by **CVD** and then ferroannealed to produce films with Aurivillius phase compn. having superior ferroelec. properties suitable for manufg. high-d. FRAMs.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L34 ANSWER 11 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:292708 HCAPLUS
DN 129:48187
TI Electrical properties of (Ba,Sr)TiO3 thin films prepared by liquid delivery **MOCVD**
AU Lee, Won-Jae; Woolcott, R. R., Jr.; Basceri, C.; Lee, Hee Young; Streiffer, S. K.; Kingon, A. I.; Yang, Doo-Young
CS Semiconductor Technology Div., Electronics and Telecommunications Research Institute (ETRI), Taejon, 305-600, S. Korea
SO Journal of the Korean Physical Society (1998), 32(Suppl., Proceedings of the 9th International Meeting on Ferroelectricity, 1997, Pt. 4), S1652-S1656
CODEN: JKPSDV; ISSN: 0374-4884
PB Korean Physical Society
DT Journal
LA English
AB The elec. properties and surface morphologies of (Ba,Sr)TiO3 thin films, with various bottom **electrode** structures, deposited by liq.-delivery metal org. **CVD** were studied. Ir and Ru films as a bottom **electrode** were prepd. onto SiO2 and polysilicon substrate structures using ion beam sputtering technique. Since the prepn. conditions of the top **electrode** influence the elec. properties of dielec. films, process conditions for Pt top **electrode** were optimized before the elec. measurement. The annealing of top **electrode** improve the leakage current of BST films and the elec. properties of BST films deposited by liq. delivery **MOCVD** was changed with the deposition temps. of Ir and Ru as well as substrate structures. Also, these variations in leakage current could be strongly related with the roughness of BST films.

L34 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:478307 HCAPLUS
DN 127:213438
TI La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3/La0.5Sr0.5CoO3 thin film heterostructures on Si using **TiN**/Pt conducting barrier
AU Yang, B.; Aggarwal, S.; Dhote, A. M.; Song, T. K.; Ramesh, R.; Lee, J. S.
CS Department of Materials and Nuclear Engineering and Center for Superconductivity Research, University of Maryland, College Park, MD, 20742, USA

SO Applied Physics Letters (1997), 71(3), 356-358
CODEN: APPLAB; ISSN: 0003-6951
PB American Institute of Physics
DT Journal
LA English
AB A high d. ferroelec. memory process flow requires the integration of conducting barrier layers to connect the drain of the pass-gate transistor to the bottom **electrode** of the ferroelec. stack. We are studying the effect of crystallinity of the **TiN**/Pt barrier layer with Si wafers on the ferroelec. properties of La0.5Sr0.5CoO3/Pb(Nb0.04Zr0.28Ti0.68)O3/La0.5Sr0.5CoO3 (LSCO/PNZT/LSCO) capacitors. Structural studies indicate complete phase purity (i.e., fully perovskite) in both epitaxial and polycryst. materials. The polycryst. capacitors show lower remnant polarization and coercive voltages. However, the retention, fatigue, and imprint characteristics are similar, indicating minimal influence of cryst. quality on the ferroelec. properties.

L36 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:79428 HCAPLUS
DN 128:122677
TI Fabrication method of semiconductor device.
IN Takuwa, Tetsuya; Yamada, Yoshiaki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10022390	A2	19980123	JP 1997-16191	19970130
	JP 3102555	B2	20001023		
	US 6107190	A	20000822	US 1997-959268	19971028
PRAI	JP 1996-111392	A	19960502		
	JP 1997-16191	A	19970130		

AB The title method involves forming an interlayer insulator BPSG film on a Si substrate, depositing a TiN or Ti film on the BPSG film by a sputtering method, forming contact holes in the films using a photoresist as a mask, forming a Ti film by a plasma **CVD** method, forming a TiN film using a thermal **CVD** method, etching back the Ti and TiN films on the BPSG film, and forming an Al wiring on the BPSG film. The sputter deposited TiN film adheres strongly to the BPSG film. Optionally, the Ti film may be formed by reducing TiCl4.

L36 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:2345 HCAPLUS
DN 128:83078
TI Growth process of thin **CVD**-aluminum films and its underlayer dependence. In-situ monitoring of reflective light intensity from depositing surface
AU Kobayashi, Akiko; Sugai, Kazumi; Sekiguchi, Atsushi; Kishida, Shyunji; Okabayashi, Hidekazu; Yako, Tadaaki; Shinzawa, Tsutomu; Okada, Osamu; Hosokawa, Naokichi; Kadokura, Hidekimi
CS Anelva Corp., Fuchu, 183, Japan
SO Aneruba Giho (1996), 1, 60-66
CODEN: ANGIFG; ISSN: 1342-2979
PB Aneruba
DT Journal
LA Japanese
AB The growth process of thin **CVD**-Al films is in-situ obsd. by a known relation of reflectivity decrease of vapor-depositing Al films along progress of the deposition in monitoring the reflected light intensity out of the Al film surface. Termination of the deposition at the max. reflection intensity gave the deposited film smooth surface in controlled quality. The min. film thickness giving surface smoothness on the deposited surface is compared to sputtered sublayers between Ti and TiN films and also compared to the effect of intermittent exposure of the sublayers to the atm. before the **CVD**. The thinnest smooth film was obtained by continuous vacuum process to give deposited Al film thickness at 60 nm on a TiN sublayer. The use of continuous vacuum process in the deposition on the TiN sublayer may be hopeful in deposition into fine grooves and contact holes at the size 0.12 .mu.m.

L36 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2002 ACS

AN 1997:799051 HCAPLUS
DN 128:64757
TI Comparison of the properties of Cu films deposited on four different types of TiN substrates
AU Shin, Young-Hoon; Lee, Chongmu
CS Department of Metallurgical Engineering, Inha University, S. Korea
SO Metals and Materials (Seoul) (1997), 3(2), 108-112
CODEN: MEMAFN; ISSN: 1225-9438
PB Korean Institute of Metals and Materials
DT Journal
LA English
AB Cu is now widely accepted as the premier replacement for Al in ULSI interconnect metalization. However, it cannot be used without a diffusion barrier since it diffuses through a SiO2 layer into the Si substrate easily. TiN is one of the potential candidates for the barrier. In this paper the properties of the Cu films deposited on four different kinds of TiN films were compared. The properties of the **CVD**-Cu film strongly depend upon the type of the TiN substrate. The Cu film with the higher quality from the viewpoint of surface roughness and thickness uniformity on the four different kinds of the TiN substrate are obtained at 180, 220, 200.degree. and 200.degree. for the TiN(TDEAT), TiN(TDEAT+NH3), TiN(TDMAT) and **TiN** (**sputtered**) substrates, resp. The Cu deposition temps. at which the Cu films with the lowest elec. resistivity are deposited 200.degree. on TiN(TDEAT), at 200.degree. on TiN(TDEAT+NH3) and TiN(TDEAT) and 180.degree. on **TiN**(**sputtered**), resp. The smoothest and flattest surface morphol. of the Cu film is obtained on TiN(TDMAT), the next on TiN(TDEAT), the third on **TiN**(**sputtered**), and the last on TiN(TDEAT+NH3) as a descending order at the Cu deposition temps. of 200.degree..

L36 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:538328 HCAPLUS
DN 122:279917
TI Semiconductor devices with multilayer interconnections
IN Tsuru, Kyohiro
PA Seiko Instr & Electronics, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06275618	A2	19940930	JP 1993-60522	19930319

AB Lower interconnections are formed by sputter deposition or **CVD** of Al alloys, and by sputter deposition of Ti and TiN films, and by patterning the films, interlayer insulator films are formed, contact holes are formed in them, where the TIN films act as etching stoppers.

L36 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:593519 HCAPLUS
DN 121:193519
TI Manufacture of semiconductor devices with laminated wirings
IN Yamashita, Yasuhiko; Inoe, Yasunori
PA Sanyo Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06140403	A2	19940520	JP 1992-290193	19921028

PI JP 06140403 A2 19940520 JP 1992-290193 19921028
AB The devices are manufd. by: (1) forming contact holes in insulating films on semiconductor substrates, (2) depositing Ti films on the holes, (3) coating the Ti films with Ti nitride films, (4) implanting O in the Ti nitride films, and (5) etching to remove the nitride films and form Al alloy films. The devices are manufd. by: (1) forming contact holes in insulating films on semiconductor substrates, (2) depositing Ti films on the holes, (3) coating the Ti films with Ti nitride films, (4) annealing the nitride films in O, and (5) successively coating the nitride films with Ti nitride films and Al alloy films. The devices are manufd. by (1) forming contact holes in insulating films on semiconductor substrates, (2) depositing Ti films on the holes, (3) implanting O and coating the films with Ti nitride films, and (4) successively coating the nitride films with Ti nitride films and Al alloy films.

L36 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:313636 HCAPLUS
DN 120:313636
TI Manufacture of semiconductor device by contact-hole burying
IN Kasai, Yoshio; Mikata, Juichi; Myazaki, Shinji; Morya, Takahiko
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 06037035	A2	19940210	JP 1992-189600	19920716

PI JP 06037035 A2 19940210 JP 1992-189600 19920716
AB The device is manufd. by (1) coating a via-hole or a contact-hole in an insulating film coated with an N- or P-type semiconductor substrate with a thin-film contg. a high melting temp. (compd.), (2) coating with forming a dopant-contg. polysilicon film thereon, and (3) etching the polysilicon film to selectively remain the polysilicon film to bury the hole.

L36 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:151603 HCAPLUS
DN 120:151603
TI Glass containing diamond film
IN Suzuki, Susumu
PA Asahi Glass Co Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 05262538	A2	19931012	JP 1992-92122	19920318

PI JP 05262538 A2 19931012 JP 1992-92122 19920318
AB The glass comprises a multilayer film contg. .gtoreq.2 layers with an outer cryst. diamond film on a glass substrate.

L36 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2002 ACS

AN 1993:638536 HCAPLUS
DN 119:238536
TI Solving process tool contamination problems
AU Busnaina, Ahmed
CS Cent. Adv. Mater. Processing, Clarkson Univ., Potsdam, NY, USA
SO Semicond. Int. (1993), 16(10), 72-5
CODEN: SITLDD; ISSN: 0163-3767
DT Journal; General Review
LA English
AB A review with 7 refs. on the use of modeling for predicting particle contamination in processes such as **CVD**, **PECVD**, sputtering, diffusion, etc. The topics include: industry significance, tool modeling, designing the process, **CVD** reactor modeling, **TiN sputtering** model, and current model developments.

L36 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2002 ACS
AN 1990:642130 HCAPLUS
DN 113:242130
TI Differential pressure sealing in continuous multichamber lines
IN Ishikawa, Yoshasu; Okago, Haruhito; Okamoto, Manabu; Nagashima, Shoji
PA Nippon Steel Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 02138467	A2	19900528	JP 1989-137365	19890601
PRAI	JP 1988-188369		19880729		

AB The title method comprises connection of .gtoreq.2 differential pressure vacuum chambers between a high- and a low-pressure vacuum chamber in a series using slits between the chambers, and control of the differential pressure between the high-pressure vacuum chamber and the differential pressure vacuum chamber adjacent thereto at a const. value with maintenance of the pressure in the latter chamber higher than that in the former chamber. The differential pressure vacuum chamber adjacent to the low-pressure vacuum chamber may be maintained at a pressure lower than that in the low-pressure vacuum chamber. Ar was supplied into the low-pressure vacuum chamber and a TiN film was formed on a moving stainless steel strip by sputtering and a SiO2 film was deposited thereon in the high-pressure vacuum chamber by **chem. vapor deposition**.

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     FILE 'REGISTRY' ENTERED AT 07:44:20 ON 28 JUN 2002
                E H2 O/MF
L1            39 S E3
L2             1 S TITANIUM/CN
L3           310 S (TI AND N)/ELS AND 2/ELC.SUB
L4             1 S ALUMINIUM/CN

     FILE 'HCAPLUS' ENTERED AT 08:03:14 ON 28 JUN 2002
L5        456567 S ELECTRODE
L6          1763 S FERROELECTRIC()CAPACITOR
L7        205781 S TITANIUM()NITRIDE OR TI()N OR TIN
L8        467757 S TI OR TITANIUM
L9       1171208 S AL OR ALUMINUM
L10         8432 S (WIR### OR LIN###)(W)(LAYER OR FILM OR COAT####)
L11        84293 S CVD OR (CHEMICAL OR CHEM)(2N)(VAPOUR OR VAPOR)(2N)DEPOSIT? OR
L12       812002 S CONDUCT######
L13       240218 S INFILTRAT? OR PENETRAT? OR PERMEAT?
L14          977 S  L5 AND L6
                E SPUTTER?/CT
                E E7+ALL/CT
                E E10-20
                E SPUTTER?/CT
                E E7+ALL/CT
L15        52831 S E10-20
L16         7603 S TIN()(SPUTTER? OR L15)
L17         7603 S TIN(W)(SPUTTER? OR L15)
L18        25268 S TITANIUM()NITRIDE
L19         8715 S (L18 OR TIN)(W)(SPUTTER? OR L15)
L20            5 S L14 AND L10
L21           16 S L14 AND L13
L22           16 S L21 NOT L20
L23            0 S L14 AND REDUC###()AGENT
L24           11 S L14 AND L2 AND L3 AND L4 AND L7 AND L8 AND L9
L25           10 S L24 NOT (L20 OR L21)
L26           45 S L14 AND (L2 OR L8) AND (L3 OR L7) AND (L4 OR L9)
L27           31 S L26 NOT (L24 OR L21 OR L20)
L28          129 S L14 AND (L3 OR L7)
L29           18 S L28 AND L15
L30           23 S L28 AND L11
L31           13 S L29 NOT (L24 OR L21 OR L20 OR 27)
L32           10 S L29 NOT (L24 OR L21 OR L20 OR L27)
L33            5 S L32 NOT (L24 OR L21 OR L20 OR L27 OR L30)
L34           12 S L30 NOT (L24 OR L21 OR L20 OR L27 OR L29)
L35            9 S TIN()SPUTTER? AND L11
L36            9 S L35 NOT (L24 OR L21 OR L20 OR L27 OR L29 OR L30)

     FILE 'WPIX, JAPIO' ENTERED AT 08:36:37 ON 28 JUN 2002
L37        24244 S (U11-C09B OR U11-C01B OR U11-C05C7 OR U11-C05C3 OR U11-C01B1)
L38          786 S L5 AND L6
L39           25 S L38 AND L10

     FILE 'HCAPLUS' ENTERED AT 08:44:29 ON 28 JUN 2002
L40           93 S L24 OR L21 OR L20 OR L27 OR L29 OR L30 OR L35
                SEL PN
L41             TRA L40 1-93 PN :      145 TERMS
L42           79 SEA L41/PN
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     FILE 'WPIX, JAPIO' ENTERED AT 08:47:24 ON 28 JUN 2002
L43          109 S L41
L44           21 S L39 NOT L43
L45           12 S L38 AND L8 AND L7 AND L9
L46            6 S L45 NOT (L43 OR L39)
L47           30 S L38 AND L8 AND L7
L48            6 S L47 AND (L11 OR L37)
L49            2 S L48 NOT (L43 OR L39 OR L45)
L50            0 S L38 AND ((TI OR TIN OR (TI()N))(W)(SPUTTER?))
L51           11 S L47 NOT (L43 OR L39 OR L45 OR L48)
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L44 ANSWER 1 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2002-308048 [35] WPIX
DNN N2002-240957 DNC C2002-089684
TI **Ferroelectric capacitor** for memory device includes two **electrodes** one of which has metal **wiring layer** embedded in contact hole.
DC L03 U11 U12 U14
PA (OKID) OKI ELECTRIC IND CO LTD
CYC 1
PI JP 2001257319 A 20010921 (200235)* 5p
ADT JP 2001257319 A JP 2000-64511 20000309
PRAI JP 2000-64511 20000309
AB JP2001257319 A UPAB: 20020603
NOVELTY - The **ferroelectric capacitor** has two **electrodes** with a ferroelectric layer formed in between. One of the **electrodes** has a metal **wiring layer** embedded in a contact hole.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for **ferroelectric capacitor** manufacturing method.
USE - Memory device.
ADVANTAGE - Since the number of etching processes is reduced, large reduction of cost and shortening of manufacturing period can be realized. The heat processing in capacitor is performed below 400 deg. C. The contact hole size turns into **electrode** size of the **ferroelectric capacitor**, thus the size of the capacitor is greatly reduced.
DESCRIPTION OF DRAWING(S) - The figure shows a section of the **ferroelectric capacitor**.
Dwg.1/4

L44 ANSWER 2 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2001-460075 [50] WPIX
DNN N2001-341170 DNC C2001-139352
TI **Ferroelectric capacitor** for ferroelectric memory, has upper **electrode** layer that includes contact layer which contains iridium or iridium oxide.
DC L03 U11 U13 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 2001127264 A 20010511 (200150)* 12p
ADT JP 2001127264 A JP 1999-309162 19991029
PRAI JP 1999-309162 19991029
AB JP2001127264 A UPAB: 20010905
NOVELTY - A ferroelectric layer (F) is formed on an **electrode** layer (E1). An upper **electrode** layer (E2) is formed on the ferroelectric layer. The upper **electrode** layer includes a contact layer (M1), a buffer layer (M2) and a **wiring layer** (M3). The contact layer includes iridium or iridium oxide.
DETAILED DESCRIPTION - The buffer layer is chosen from among group consisting of thallium, lead, rubidium, cesium, tin, ruthenium, rhodium, osmium, niobium, vanadium, bismuth, molybdenum, chrome and rhenium or its oxides. INDEPENDENT CLAIMS are also included for the following:
(a) **Ferroelectric capacitor** manufacturing method;
(b) Ferroelectric memory
USE - For backup power supply of ferroelectric memory e.g. ferroelectric random access memory (FRAM).
ADVANTAGE - Eliminates raise of **electrode** resistance and

inferior contact. Improves contact yield by reducing contact resistance by using iridium **electrode**.

DESCRIPTION OF DRAWING(S) - The figure shows the conceptual diagram of principal portion cross section component of dielectric capacitor. (Drawing includes non-English language text).

Electrode layers E1,E2

Ferroelectric layer F

Contact layer M1

Buffer layer M2

Wiring layer M3

Dwg.1/14

L44 ANSWER 3 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2001-303293 [32] WPIX
DNN N2001-217916
TI Ferroelectric random access memory has insulation film formed on etching stopper film which is formed on surface of **ferroelectric capacitor** on which pair of **electrodes**, ferroelectric film are laminated.
DC U11 U12 U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 2000349247 A 20001215 (200132)* 10p
ADT JP 2000349247 A JP 1999-158271 19990604
PRAI JP 1999-158271 19990604
AB JP2000349247 A UPAB: 20010611

NOVELTY - Etching stopper film (13) made of titanium oxide cover. The capacitor made of ferroelectric thin film (11) formed between pair of **electrodes** (10,12). Insulation film (15) made of silicon oxide is formed above stopper film (13). Thickness of lower **electrode** (10), ferroelectric film (11), upper **electrode** (12) are same as the **wiring layer** (18).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for ferroelectric random access memory manufacturing method.

USE - Ferroelectric random access memory.

ADVANTAGE - Degradation of electrical property is prevented. Reliability of ferroelectric film is increased, manufacturing of memory is simplified.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device.

Electrodes 10,12

Ferroelectric thin film 11

Etching stopper film 13

Insulation film 15

Wiring layer 18

Dwg.1/8

L44 ANSWER 4 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2000-191817 [17] WPIX
DNN N2000-142952
TI **Ferroelectric capacitor** for ferroelectric random access memory, has **wiring layer** formed on upper **electrode** via contact hole formed on insulating films.
DC U11 U12 U13 U14
IN SHUTO, S
PA (TOKE) TOSHIBA KK
CYC 2
PI JP 2000036568 A 20000202 (200017)* 7p

US 6313491 B1 20011106 (200170)
ADT JP 2000036568 A JP 1998-202979 19980717; US 6313491 B1 US 1999-354101 19990715
PRAI JP 1998-202979 19980717
AB JP2000036568 A UPAB: 20000405
NOVELTY - A **ferroelectric capacitor** is formed on surface of semiconductor substrate (11) via the first insulating film. A **wiring layer** (28) is formed on surface of second and third insulating layers so as to cover the **ferroelectric capacitor** and the **wiring layer**. The **wiring layer** (34) is formed on upper **electrode** (23) via contact hole formed on second and third insulating layers. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for manufacturing method of semiconductor memory.
USE - For ferroelectric random access memory.
ADVANTAGE - The problem of wiring material fusing by annealing of **ferroelectric capacitor** does not arise. The process and the implanting of contact hole are simple, thus miniaturization is attained. DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of manufacturing process of semiconductor memory. (11) Semiconductor substrate; (23) Upper **electrode**; (28) **Wiring layer**; (34) **Wiring layer**.
Dwg.1/4

L44 ANSWER 5 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 2000-132642 [12] WPIX
DNN N2000-100403
TI **Wiring layer** formation structure for ferroelectric memory - has upper **electrode** of **wiring layer** and **ferroelectric capacitor** which are overlapped mutually such that one end of **wiring layer** does not exist among upper **electrode**.
DC U14
IN HIRANO, H; HONDA, T
PA (MATE) MATSUSHITA ELECTRONICS CORP; (HIRA-I) HIRANO H; (HOND-I) HONDA T
CYC 2
PI JP 2000004000 A 20000107 (200012)* 7p
JP 3236262 B2 20011210 (200203) 7p
US 2002008263 A1 20020124 (200210)
ADT JP 2000004000 A JP 1998-167857 19980616; JP 3236262 B2 JP 1998-167857 19980616; US 2002008263 A1 US 1999-333049 19990615
FDT JP 3236262 B2 Previous Publ. JP 2000004000
PRAI JP 1998-167857 19980616
AB JP2000004000 A UPAB: 20000308
NOVELTY - The memory cell transistor and **ferroelectric capacitor** are formed over layer insulation film (15). A **wiring layer** (20) is formed on layer insulation film (19). The upper **electrode** of **wiring layer** and **ferroelectric capacitor** are overlapped mutually such that one end of **wiring layer** does not exist among upper **electrode**. DETAILED DESCRIPTION - A **ferroelectric capacitor** having a ferroelectric film (17), is interposed between upper and lower **electrodes** (TE,16). A memory cell transistor controls supply of voltage of upper **electrode** (TE) of **ferroelectric capacitor**.
USE - For ferroelectric memory used in portable terminal, IC card.
ADVANTAGE - Characteristics, such as retention of **ferroelectric capacitor** resulting from the stress of

wiring layer opposing to **ferroelectric capacitor** are improved. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of ferroelectric memory. (15) Over layer insulation film; (TE,16) Upper and lower **electrodes**; (19) Layer insulation film; (20) **Wiring layer**; (17) Ferroelectric film.
Dwg.2/5

L44 ANSWER 6 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1999-246681 [21] WPIX
DNN N1999-183787 DNC C1999-072216
TI Ferroelectric device for semiconductor integrated circuit.
DC L03 U11 U13 U14
IN JUDAI, Y
PA (MATE) MATSUSHITA ELECTRONICS CORP; (JUDA-I) JUDAI Y
CYC 27
PI EP 911879 A1 19990428 (199921)* EN 9p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 11126876 A 19990511 (199929) 5p
US 2002000588 A1 20020103 (200207)
US 2002047111 A1 20020425 (200233)
ADT EP 911879 A1 EP 1998-120016 19981022; JP 11126876 A JP 1997-293046 19971024; US 2002000588 A1 US 1998-177038 19981022; US 2002047111 A1 Div ex US 1998-177038 19981022, US 2001-990474 20011121
PRAI JP 1997-293046 19971024
AB EP 911879 A UPAB: 19990603
NOVELTY - A semiconductor device comprises a **ferroelectric capacitor** (3) on a circuit board, covered by insulating film (4) and with wiring connection (5) to a capacitor **electrode**. There is a protection film (6) and an extensional synthetic stress working in a surface direction of the ferroelectric thin film.
DETAILED DESCRIPTION - A semiconductor device comprises a **ferroelectric capacitor** (3) on a circuit board (1, 2) having a thin film (3c) between **electrodes** (3a, b), an insulating film (4) over the board over which is metallic wiring (5a, b) connected to an **electrode**. A surface protection film (6) covers the insulation and **wiring films** and there is an extensional synthetic stress working in a surface direction of the ferroelectric thin film.
An INDEPENDENT CLAIM is also included for the production of the above semiconductor device in which the insulating film is formed by ozone-activated TEOS-CVD, the wiring has two layers, the bottom being titanium nitride and the top of aluminum.
USE - As ferroelectric nonvolatile memories in semiconductor devices.
ADVANTAGE - The extensional stress overcomes the problems of performance deterioration caused by compressive stress and improves the residual dielectric polarization and leak current characteristics.
DESCRIPTION OF DRAWING(S) - The drawing shows a sectional view of the capacitor.
Ferroelectric capacitor 3
Insulating film 4
Wiring films 5
Protective film 6
Dwg.1/4

L44 ANSWER 7 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1998-512639 [44] WPIX

DNN N1998-400349 DNC C1998-154311
TI Capacitor for ferroelectric memory - has thin upper and lower **electrodes** in between which insulating film is formed and whose periphery is covered by titanium oxide or titanium nitriding film.
DC L03 U11 U12 U13 U14
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 10223852 A 19980821 (199844)* 7p
ADT JP 10223852 A JP 1997-20577 19970203
PRAI JP 1997-20577 19970203
AB JP 10223852 A UPAB: 19981104
The capacitor (14) is formed on a semiconductor substrate (11) which has a lower metal thin **electrode** (14a) and a thin metal upper **electrode** (14c). A thin capacitive insulating film (14b) is formed between the lower and upper **electrodes**. A Ti oxide on Ti nitriding film (15) covers the peripheral surface of the capacitor.
A second connection hole (13b) is formed in the portion of the Ti oxide film, corresponding to the upper **electrode**. A **wiring layer** (16) is formed on the sides and base of the first and second holes continuously. A Ti nitriding **wiring layer** (16a) and a thin metal **wiring layer** (16b) are sequentially formed in the **wiring layer**.
USE - For semiconductor device.
ADVANTAGE - Offers **ferroelectric capacitor** having desired electrical property.
Dwg.1/4

L44 ANSWER 8 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-441378 [41] WPIX
DNN N1997-367285
TI Semiconductor device for memory unit - has access transistor which is connected to bit-line above upper **electrode** layer of **ferroelectric capacitor**, based on operation potential of word-line.
DC U12
PA (SONY) SONY CORP
CYC 1
PI JP 09199678 A 19970731 (199741)* 6p
ADT JP 09199678 A JP 1996-7265 19960119
PRAI JP 1996-7265 19960119
AB JP 09199678 A UPAB: 19971013
The device includes a **ferroelectric capacitor** (6) enclosing an upper **electrode** layer (6c), a ferroelectric substance layer (6b) and a plate **electrode** layer (6a). An access transistor (AT) is provided which is connected to a bit-line (11) above the upper **electrode** layer, depending upon the operation potential of a word-line (7).
A connection **wiring layer** (13) is thus formed between the diffusion layer of the access transistor and the bit-line.
ADVANTAGE - Reduces memory-cell size. Etches connection hole of access transistor diffusion layer, **wiring layer** of bit-line splicing and bit-line, easily. Improves **wiring layer** coverage in connection hole.
Dwg.1/9

L44 ANSWER 9 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-383338 [35] WPIX
DNN N1997-319154

TI Ferroelectric memory device - has bit line configured by electrical connection of **ferroelectric capacitor** **electrode** with diffusion layer of driving transistor.
DC U11 U13 U14
PA (SONY) SONY CORP
CYC 1
PI JP 09167796 A 19970624 (199735)* 7p
ADT JP 09167796 A JP 1995-347814 19951215
PRAI JP 1995-347814 19951215
AB JP 09167796 A UPAB: 19970828
The device has a **ferroelectric capacitor** (11) whose **electrode** terminal (32) is electrically connected with a diffusion layer (24) of a driving transistor (12) through a **wiring layer** (41).
By this electrical coupling, a bit line (14) is configured which is superimposed on the **wiring layer** in the 3D manner.
ADVANTAGE - Aims at size reduction of memory device. Improves integration density of memory. Reduces mfg cost.
Dwg.1/8

L44 ANSWER 10 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-287077 [26] WPIX
DNN N1997-237791
TI Semiconductor memory with **ferroelectric capacitor** - has strip-shaped wiring with electrically-conductive strip-shaped layer containing two or more upper **electrodes** that are to be electrically connected.
DC U13 U14
PA (ROHL) ROHM CO LTD
CYC 1
PI JP 09107077 A 19970422 (199726)* 11p
ADT JP 09107077 A JP 1995-261401 19951009
PRAI JP 1995-261401 19951009
AB JP 09107077 A UPAB: 19970626
The memory (20) has a **ferroelectric capacitor** (C1) composed of a lower **electrode** (24) with a conductive material, a ferroelectric interface layer (26) and an upper **electrode** (32) with another conductive material. The upper **electrodes** of two or more **ferroelectric capacitors** are electrically connected.
A strip-shaped wiring has an electrically-conductive strip-shaped layer that contains two or more upper **electrodes** that are to be electrically connected.
ADVANTAGE - Does not require separate wiring for electrically connecting two or more upper **electrodes** by using strip-shaped wiring with electrically-conductive strip-shaped layer that contains two or more upper **electrodes** to be electrically connected. Does not require large space for connecting upper **electrode** and upper wiring. Prevents disconnecting surface of lower **electrode** from contacting strip-shaped wiring of lower **electrode** even if disconnecting surface of lower **electrode** is not covered by interface layer. Prevents deterioration of semiconductor component since ferroelectric layer does not directly contact silicon oxide film of lower conductive material layer.
Dwg.1/13

L44 ANSWER 11 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1997-052645 [05] WPIX

DNN N1997-043137 DNC C1997-017593
TI Integrated circuit device for **ferroelectric capacitor electrodes** - comprising substrate, layer sequence including buffer layer(s) of layered super-lattice material and metal **wiring layer**.
DC L03 U11 U12 U14
IN AZUMA, M; CUCHIARO, J D; PAZ, DE ARAUJO C A
PA (MATE) MATSUSHITA ELECTRONICS CORP; (SYME-N) SYMETRIX CORP; (MATU) MATSUSHITA DENKI KK
CYC 23
PI WO 9641375 A1 19961219 (199705)* EN 34p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CA CN JP KR SG
EP 834196 A1 19980408 (199818) EN
R: DE FR GB IT NL
CN 1199506 A 19981118 (199914)
TW 347577 A 19981211 (199920)
JP 11511293 W 19990928 (199952) 37p
KR 99022075 A 19990325 (200023)
ADT WO 9641375 A1 WO 1996-US9100 19960606; EP 834196 A1 EP 1996-918175 19960606, WO 1996-US9100 19960606; CN 1199506 A CN 1996-194607 19960606; TW 347577 A TW 1996-110426 19960827; JP 11511293 W WO 1996-US9100 19960606, JP 1997-501501 19960606; KR 99022075 A WO 1996-US9100 19960606, KR 1997-708554 19971128
FDT EP 834196 A1 Based on WO 9641375; JP 11511293 W Based on WO 9641375; KR 99022075 A Based on WO 9641375
PRAI US 1995-473432 19950607
AB WO 9641375 A UPAB: 19970129
Integrated circuit (IC) device comprises: (i) a substrate; (ii) a layer sequence consisting of material interposed between substrate (i) and metal **wiring layer** (iii) including buffer layer(s) of layered super-lattice material (SLM), and being free of additional **wiring layers**; and (iii) a metal **wiring layer**. Also claimed is a method of making the IC device comprising: (a) providing a substrate having a non-metallic uppermost surface; (b) depositing a layered SLM precursor on top of the substrate; and (c) depositing an **electrode** over the layered SLM.
USE - For **electrodes** of **ferroelectric capacitors**.
ADVANTAGE - Materials form thin-film layers that have high polarisation, compatibility and reliability without cracking, peeling, diffusion contamination or surface irregularity.
Dwg.1/5

L44 ANSWER 12 OF 21 WPIX (C) 2002 THOMSON DERWENT
AN 1992-097110 [12] WPIX
DNN N1992-072600 DNC C1992-045114
TI Semiconductor device contg. ferroelectric film or polycrystalline silicon - has protective hydrogen , oxygen , moisture and electromagnetic shielding film of titanium (oxy) nitride.
DC L03 U11 U13 U14
IN FUJISAWA, A; TAKENAKA, K
PA (RAMT-N) RAMTRON INT CORP; (SHIH) SEIKO EPSON CORP
CYC 13
PI WO 9203849 A 19920305 (199212)* 21p
RW: AT CH DE DK ES GB GR LU
W: US
JP 04102367 A 19920403 (199220) 8p

EP 514547 A1 19921125 (199248) EN 12p

AB WO 9203849 A UPAB: 19940727
A semiconductor (1) device having a ferroelectric film or a polycrystalline Si- gate as an element is furnished with a humidity-resistant hydrogen barrier film (2) formed on at least the upper area covering the element. The film (2) is formed on the ferroelectric film or the polycrystalline Si- gate by a film forming method that releases no H2. A Rust-preventing SiN. film can be formed over the film (2). The film (2) can be TiN or TiON.

Producing the semi conductor device (1) comprises (i) forming an interlayer insulation film by a film-forming method that releases no H2 after forming the ferroelectric film or the polycrystalline Si- gate, and (ii) forming a humidity -resistant H2 barrier film, by a film-forming method that releases no H2, over at least the area covering the element and, opt., forming a rust-preventing film over the H2 barrier film. Semiconductor memory or a CMOS semiconductor integrated circuit is produced using the invented semiconductor device.

ADVANTAGE - Since the TiN film is dense and electrically conductive,it works as not only a protecting film against H2 and H2O but also as an electromagnetic shield. TiON has a higher H2 barrier characteristic than TiN and is insulative hence the number of interlayer insulating films can be decreased. Widely useful for semiconductor integrated circuits.

In an example, a typical semiconductor memory chip having a gate insulation film, a thick LOCOS 6 as the active region of MOS formed on a p-type semiconductor, and a polycrystalline Si- gate, an interlayer insulation film (SiO2 or SiN) was formed by a CVD method. Over this interlayer insulating film, a secondary SiN interlayer insulation film, plate **electrodes**, an inner Al **wiring layer**
etc. were formed.
1/6
Dwg.1/6

L44 ANSWER 13 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 2001-127264 JAPIO
TI **FERROELECTRICS CAPACITOR**, MANUFACTURING METHOD THEREFOR, AND FERROELECTRICS MEMORY
IN HIDAKA OSAMU
PA TOSHIBA CORP
PI JP 2001127264 A 20010511 Heisei
AI JP1999-309162 (JP11309162 Heisei) 19991029
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide a **ferroelectrics capacitor** wherein the **electrode** of a **wiring layer** formed on the **ferroelectrics capacitor** is prevented from being oxidized, as well as its manufacturing method and a ferroelectrics memory.
SOLUTION: A buffer layer comprising a metal element which is lower in a specific resistance of oxide and, easier to be oxidized than a contact layer or **wiring layer** is provided, so that the oxygen dissociated from an ferroelectric oxide and a contact layer contacting it is surely adsorbed, and a barrier layer of metal wiring is assuredly prevented from being oxidized. As a result, rising of an **electrode** resistance or defective contact is settled. Even with an iridium **electrode** which is easy to release oxygen, a contact resistance is lowered with a contact yield significantly improved, and further, a repeated writing/reading characteristics is excellent as a ferroelectrics

memory.
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L44 ANSWER 14 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 2000-349247 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN INOUE HISAYA; TAKEUCHI TSUNEO; HAYASHI YOSHIHIRO
PA NEC CORP
PI JP 2000349247 A 20001215 Heisei
AI JP1999-158271 (JP11158271 Heisei) 19990604
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve memory characteristic and reliability of a semiconductor device, which is provided with a ferroelectric substance memory part and has a multilayered wiring structure.
SOLUTION: An etching stopper film 13 is adhered to the surface of a ferroelectric substance capacitor, composed of a lower **electrode** 10, a ferroelectric substance film 11 and an upper **electrode** 12, and an interlayer insulating film 15 of a different kind is formed on the etching stopper film 13. In a semiconductor device, having a ferroelectric substance capacitor and a multilayered wiring structure, the ferroelectric substance capacitor and first **wiring layer** 18 and 19 are formed on an interlayer insulating film 18, so that the film thickness of the ferroelectric substance capacitor is made the same as that of the first **wiring layer**. Furthermore, in a memory cell having a **ferroelectric capacitor**, a bit line 16 and a plate line 17 are arranged above the ferroelectric substance capacitor with the interlayer insulation film 18 interposed, and the bit line and plate line are arranged at high density.
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L44 ANSWER 15 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 2000-004000 JAPIO
TI FERROELECTRIC MEMORY DEVICE
IN HIRANO HIROSHIGE; HONDA TOSHIYUKI
PA MATSUSHITA ELECTRON CORP
PI JP 2000004000 A 20000107 Heisei
AI JP1998-167857 (JP10167857 Heisei) 19980616
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To improve a ferroelectric memory device in reliability, wherein the ferroelectric memory device is provided with a **ferroelectric capacitor** equipped with a ferroelectric film interposed between a lower **electrode** and an upper **electrode** and arranged in memory cells.
SOLUTION: Memory cell transistors where word lines serve as gates are provided in an active region OD, and a **ferroelectric capacitor** composed of a lower **electrode**, a ferroelectric film, and an upper **electrode** TE is provided on an element isolating region. A first **wiring layer** is composed of a storage wiring 20 which connects the upper **electrode** TE to the one impurity diffusion layer of the memory cell transistor and a bit line BL connected to the other impurity diffusion layer of the memory cell transistor. In a plan view, the storage wiring 20 intersects only one side of the upper **electrode** TE, and the bit line BL does not overlap with the upper **electrode** TE. By this setup, a **ferroelectric capacitor** can be enhanced in properties such as retention caused by stress imposed on it by a first **wiring layer**.
COPYRIGHT: (C)2000,JPO

L44 ANSWER 16 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1999-040768 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT AND ITS MANUFACTURE
IN KANETANI HIROYUKI; HIDAKA OSAMU; OKUWADA HISAMI; MOCHIZUKI HIROSHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 11040768 A 19990212 Heisei
AI JP1997-192168 (JP09192168 Heisei) 19970717
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 2
AB PURPOSE: TO BE SOLVED:To provide a structure where the characteristics of a ferroelectric film will not deteriorate in an LSI where a nonvolatile dielectric memory (FRAM) exexit with other devices, by facilitating the machining of a Pt **electrode** and that of a capacitor, reducing the number of processes for forming the lower **electrode** of a capacitor part and the **wiring layer** of other devices, reducing the level difference between devices, and facilitating the formation of wiring.
CONSTITUTION: ructure has a first **electrode** 3a that is buried into a first groove being dug at a first insulation film that is formed on a semiconductor substrate and whose surface is flattened, a second insulation film being deposited on the first insulation film, a ferroelectric film 5a and a second **electrode** 6a that are successively deposited into a second groove being dug at the second insulation film corresponding to the upper part of the first **electrode** 3a and then whose surface is flattened. Then, it has a **ferroelectric capacitor** part that is constituted of the first **electrode** 3a, the ferroelectric film 5a, and the second **electrode** 6a.

L44 ANSWER 17 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1998-223852 JAPIO
TI FERROELECTRIC MEMORY DEVICE AND MANUFACTURE THEREOF
IN SOSHIRO YUUJI
PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
PI JP 10223852 A 19980821 Heisei
AI JP1997-20577 (JP09020577 Heisei) 19970203
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 8
AB PURPOSE: TO BE SOLVED:To prevent hydrogen from penetrating into a capacitor in a ferroelectric memory device.
CONSTITUTION: rroelectric capacitor 14 composed of a lower **electrode** 14a of metal thin film, a capacitor insulating film 14b of ferroelectric thin film, and an upper **electrode** of metal thin film is formed on a semiconductor substrate 11. The upside and side face of the **ferroelectric capacitor** 14 are covered direct with a Ti oxide film 15. A first connection hole 13a which exposes the upside of the semiconductor substrate 11 located between a transistor 12 and the **ferroelectric capacitor** 14 and a second connection hole 13b which makes the upside of the upper **electrode** 14e exposed are provided to an interlayer insulating film 13, the semiconductor substrate 1 and the upper **electrode** 14c are electrically connected together, and a multilayered **wiring layer** 16 composed of a first **wiring layer** 16a of Ti nitride and a second **wiring layer** 16b formed of metal thin film is provided.

L44 ANSWER 18 OF 21 JAPIO COPYRIGHT 2002 JPO

AN 1997-199678 JAPIO
TI SEMICONDUCTOR DEVICE
IN NAIKI TADAHACHI
PA SONY CORP, JP (CO 000218)
PI JP 09199678 A 19970731 Heisei
AI JP1996-7265 (JP08007265 Heisei) 19960119
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 7
AB PURPOSE: TO BE SOLVED:To improve the coverage of a **wiring layer** in a connection hole by reducing a memory cell size and easily etching the connection hole.
CONSTITUTION: vice has a **ferroelectric capacitor** 6 and an access transistor AT for connecting an upper **electrode** layer 6c of the **ferroelectric capacitor** 6 to a bit line 11 according to the potential of a word line so that it can operate and connects a diffusion layer 2 of the access transistor AT and the bit line 11 via a connection diffusion layer 13 which is different from the bit **line layer** 11, thus forming the bit line and a connection hole for the connection **wire layer** 13 in the cell in self-alignment manner for the word line and hence reducing the memory cell size.

L44 ANSWER 19 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1996-186234 JAPIO
TI FERROELECTRIC MEMORY
IN TANABE NOBUHIRO
PA NEC CORP, JP (CO 000423)
PI JP 08186234 A 19960716 Heisei
AI JP1995-304 (JP07000304 Heisei) 19950105
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 7
AB PURPOSE: To reduce the area of a memory cell without complicating the process as compared with a conventional art.
CONSTITUTION: A field effect transistor and a field oxide film 3 are made on a substrate. Thereon, a bit line 4 is made, being connected to a diffused layer 1-1 common to two field effect transistors. On the bit line 4 is a **ferroelectric capacitor** consisting of a lower **electrode** 5, a ferroelectric film 6, and an upper **electrode** 7 made with a flattened interlayer insulating film between. And, the upper **electrode** 7 is connected to the diffused layer 1-2 not common, by a **wiring layer** 8, and beside several **ferroelectric capacitor** connected to the two transistors having a common diffused layer 1-1 are not arranged symmetrically about the common diffused layer 1-1, and only the minimum insulating film for the **ferroelectric capacitor** and the connection by the wiring not to electrically short-circuit with each other exists in the section excluding the connection by the **ferroelectric capacitor** and the wiring.

L44 ANSWER 20 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1995-211862 JAPIO
TI METAL WIRING AND CAPACITOR STRUCTURE USING METAL WIRING AND ITS MANUFACTURE
IN TANABE NOBUHIRO; HAYASHI YOSHIHIRO; KUNIO TAKEMITSU; MATSUKI TAKEO
PA NEC CORP, JP (CO 000423)
PI JP 07211862 A 19950811 Heisei
AI JP1994-5681 (JP06005681 Heisei) 19940124
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No.

8

AB PURPOSE: To provide a highly reliable **ferroelectric capacitor** by preven-ting the formation of a large step difference when a metal wiring is made thick in order to avoid the generation of the high resistance of the metal **electrode wiring layer** of the **ferroelectric capacitor** caused by the reduction of the area of a memory cell accompanied by the high-density integration of the memory in a ferroelectric memory.
CONSTITUTION: A metallic ground **electrode** wiring 2 is embedded in a layer insulating film 6 having the flat surface, which is formed on a semiconductor substrate. A metal film 3, a ferroelectric film 4 and an upper metal wiring 5 are formed at the upper part of a structure, where the upper layer of the metallic ground **wiring layer** appears. The structure of the **ferroelectric capacitor** such as this is obtained.

L44 ANSWER 21 OF 21 JAPIO COPYRIGHT 2002 JPO
AN 1995-115141 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE
IN KURODA KENICHI
PA HITACHI LTD, JP (CO 000510)
PI JP 07115141 A 19950502 Heisei
AI JP1993-282008 (JP05282008 Heisei) 19931014
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 5

AB PURPOSE: To enable an FRAM of 1-MOS multi-capacitor type to be lessened in cost and stabilized in operating characteristics.
CONSTITUTION: In an FRAM of 1-MOS multi-capacitor type, part or all of a certain number of **ferroelectric capacitors** whose lower **electrodes** are connected together in common are so formed to overlap the upper layer of corresponding selection MOSFETs QN0 and QN1, the **ferroelectric capacitors** and sub-data lines d000 and d100 serving as the lower **electrodes** of the capacitors connected together in common are formed above a metal **wiring layer** of data line or the like after a wiring is formed an processed. By this setup, selection MOSFETs and a prescribed number of corresponding **ferroelectric capacitors** are three-dimensionally formed, a memory array can be enhanced in layout efficiency, and a thermal treatment carried out in a wiring forming process can be restrained from affecting a **ferroelectric capacitor** in holding characteristics.

L46 ANSWER 1 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2002-178006 [23] WPIX
DNC C2002-054860
TI **Ferroelectric capacitor** capable of increasing interface feature between ferroelectric film and upper **electrode** and method for forming the same.
DC L03 U12
IN KIM, N G; YUM, S J
PA (HYNI-N) HYNIX SEMICONDUCTOR INC
CYC 1
PI KR 2001061365 A 20010707 (200223)* 1p
ADT KR 2001061365 A KR 1999-63859 19991228
PRAI KR 1999-63859 19991228
AB KR2001061365 A UPAB: 20020411
NOVELTY - A **ferroelectric capacitor** of an FRAM device is provided to restrain increase of current leakage by enhancing interface features of a ferroelectric film and a capacitor upper **electrode**.

DETAILED DESCRIPTION - A **ferroelectric capacitor** is constituted by a lower **electrode** on a semiconductor substrate(10), a ferroelectric film(16) and an upper **electrode**. An oxide film(17) is formed on the ferroelectric film to prevent decrease of the short key barrier height of the ferroelectric film(16) and the upper **electrode**. The oxide film(17) is made of TEOS SiO2 or SiON. The ferroelectric film(16) is made of SBT or SBTN, and the lower **electrode** and the upper **electrode** are made of Pt films. An anti-diffusion film(21) and a metal film(22) are made of **Ti** or **TiN** to form a metal line for connecting a transistor and the **ferroelectric capacitor**. The metal film(22) is coated with an **Al** film.
Dwg.1/10

L46 ANSWER 2 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2002-074731 [10] WPIX
DNN N2002-055136 DNC C2002-022174
TI Manufacture of ferroelectric random access memory device comprises forming **ferroelectric capacitor** structure, insulating layer and photoresist pattern, etching insulating layer and forming metal interconnection pattern.
DC L03 U11
IN KWON, O S; PARK, C R; SUL, Y S; KWON, O; PARK, C; SEOL, Y
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYNI-N) HYNIX SEMICONDUCTOR INC; (KWON-I) KWON O; (PARK-I) PARK C; (SEOL-I) SEOL Y
CYC 3
PI US 2001048622 A1 20011206 (200210)* 11p
JP 2002026287 A 20020125 (200211) 6p
KR 2001109610 A 20011212 (200237)
ADT US 2001048622 A1 US 2001-867419 20010531; JP 2002026287 A JP 2001-148620 20010518; KR 2001109610 A KR 2000-29642 20000531
PRAI KR 2000-29642 20000531
AB US2001048622 A UPAB: 20020213
NOVELTY - Manufacture of a ferroelectric random access memory device comprises forming a **ferroelectric capacitor** structure having a buffer on an insulating layer, bottom and top **electrodes**, and a capacitor thin film; forming a second insulating layer and a photoresist pattern; etching the second insulating layer and exposed part

of capacitor thin film; and forming metal interconnection pattern.

DETAILED DESCRIPTION - Manufacture of a ferroelectric random access memory (FeRAm) device comprises

(a) preparing an active matrix (210) incorporating a substrate, a transistor, an isolation region and a first insulating layer (212);

(b) forming a **ferroelectric capacitor** structure comprising a buffer (214) formed on the insulating layer, a bottom **electrode** (216) formed on the buffer, a capacitor thin film (218) formed on the bottom **electrode**, and a top **electrode** (220) formed on the capacitor thin film;

(c) forming a second insulating layer on the top **electrode**, the capacitor thin film and the first insulating layer;

(d) forming a photoresist pattern on the second insulating layer that exposes a first portion of the second insulating above the top **electrode** and exposes a second portion of the second insulating layer above the bottom **electrode**;

(e) etching the first portion of the second insulating layer to expose a portion of the top **electrode**, forming a storage node contact hole and etching the second portion of the second insulating layer to expose a portion of the capacitor thin film;

(f) etching the exposed portion of the capacitor thin film to form a cell plate contact hole; and

(g) forming a metal interconnection pattern over the second insulating layer and into the storage node contact hole and the cell plate contact hole.

USE - For manufacturing FeRAM device.

ADVANTAGE - The inventive method produces FeRAM devices utilizing a simplified method of manufacturing the **ferroelectric capacitors** incorporated in the FeRAM. It produces the **ferroelectric capacitor** structure using simplified process that preserves the electrical properties of the cell plate contact.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of FeRAM device incorporating a **ferroelectric capacitor**.

Active matrix 210
First insulating layer 212
Buffer 214
Bottom **electrode** 216
Capacitor thin film 218
Top **electrode** 220
Dwg.2A/2

L46 ANSWER 3 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 2001-388838 [41] WPIX
DNN N2001-285913 DNC C2001-118540
TI Formation of barrier layer in ferroelectric memory, involves forming local interconnect metal layer before forming continuous barrier layer.
DC L03 U11
IN HICKERT, G
PA (RAMT-N) RAMTRON INT CORP
CYC 1
PI US 6242299 B1 20010605 (200141)* 15p
ADT US 6242299 B1 US 1999-283166 19990401
PRAI US 1999-283166 19990401
AB US 6242299 B UPAB: 20010724
NOVELTY - Formation of a barrier layer in a ferroelectric memory involves local interconnect metal layer before forming a continuous barrier layer.

The local interconnect metal layer is formed between the top **electrode** of a **ferroelectric capacitor** and a source/drain transistor contact.

DETAILED DESCRIPTION - Formation of a barrier layer in a ferroelectric memory having top and bottom **ferroelectric capacitor electrodes** (26, 22) and first and second source/drain transistor contacts (14) comprises forming a first oxide layer on the top surface of the ferroelectric memory. Contacts are formed through the first oxide layer to the top and bottom **electrodes**, and first and second source/drain contacts. A local interconnect metal layer (40) is patterned on the bottom **electrode** and second source/drain contact, and between the top **electrode** and the first source/drain contact. A continuous barrier layer (42) is directly formed on the local interconnect metal layer. A second oxide layer (44) is formed on the continuous barrier layer. Contacts (46) are formed through the second oxide layer and the barrier layer to the bottom **electrode** and second source/drain.

USE - For forming barrier layer e.g., silicon nitride layer, in ferroelectric memory.

ADVANTAGE - The inventive method minimizes damage to the **ferroelectric capacitor** and improves electrical performance of the ferroelectric memory. It avoids the loss of barrier integrity resulting from contact cuts through the barrier layer, as is the case with prior art barriers formed directly on the capacitor stack.

DESCRIPTION OF DRAWING(S) - The figures illustrate the formation of the barrier layer.

Source/drain transistor contacts 14

Ferroelectric capacitor electrodes 22, 26

Local interconnect metal layer 40

Continuos barrier layer 42

Second oxide layer 44

Contacts 46

Dwg.5, 6/13

L46 ANSWER 4 OF 6 WPIX (C) 2002 THOMSON DERWENT

AN 2000-389485 [34] WPIX

DNN N2000-291667 DNC C2000-118461

TI Semiconductor device capable of preventing ohmic resistance increase between contact region and metallic **electrode** includes an oxidation preventive layer which covers the contact region.

DC L03 U11 U12 U13 U14

IN KAGEYAMA, S; SAMESHIMA, K

PA (ROHL) ROHM CO LTD

CYC 26

PI EP 1011144 A1 20000621 (200034)* EN 17p

R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

JP 2000183296 A 20000630 (200037) 8p

ADT EP 1011144 A1 EP 1999-310112 19991215; JP 2000183296 A JP 1998-357819 19981216

PRAI JP 1998-357819 19981216

AB EP 1011144 A UPAB: 20000718

NOVELTY - An oxidation preventive layer (15, 17) covers contact region (13).

DETAILED DESCRIPTION - A semiconductor device comprises: a contact region (13) formed in a reducing atmosphere on a substrate (3); a ferroelectric layer (19b) formed on the substrate (3); and an oxide layer

formed on the contact region or ferroelectric layer. An oxidation preventative layer (15, 17) is formed to cover the contact region.

INDEPENDENT CLAIMS are also included for the following:

(a) a semiconductor device comprising:

(i) a tungsten plug (13) formed in a reducing atmosphere on a substrate;

(ii) a **titanium** layer formed (15) on the tungsten plug;

(iii) a **titanium nitride** layer (17) formed on the **titanium** layer;

(iv) a first oxide layer (18) formed on the **titanium nitride** layer;

(v) a ferroelectric layer (19b) formed on the first oxide layer and

(vi) a second oxide layer (21) formed on the ferroelectric layer and on the tungsten plug;

(b) a semiconductor device comprising:

(i) a tungsten plug (13) formed in a reducing atmosphere on a substrate;

(ii) a **titanium** layer (15) formed on the tungsten plug;

(iii) a **titanium nitride** layer (17) formed on the **titanium** layer;

(iv) a ferroelectric layer (19b) formed on the substrate; and

(v) an oxide layer (21) formed on the ferroelectric layer and on the tungsten plug; and

(c) methods of manufacturing a semiconductor device.

USE - None given.

ADVANTAGE - The semiconductor device is capable of preventing the ohmic resistance between the tungsten plug and the metallic **electrode** from increasing even if an oxide film is formed on the tungsten plug.

DESCRIPTION OF DRAWING(S) - The diagram illustrates an embodiment of a semiconductor device.

Semiconductor device 1

P-type substrate 3

N-type region 5

Gate **electrode** 6

Boro-phospho-silicate glass layer 7

Lower **titanium** layer 9

Lower **titanium nitride** layer 11

Tungsten plug 13

Upper **titanium** layer 15

Upper titanium nitride layer 17

Undoped silicate glass layer 18

Ferroelectric capacitor 19

Phospho-silicate glass layer 21

Aluminum electrode 23

Dwg.1/8

L46 ANSWER 5 OF 6 WPIX (C) 2002 THOMSON DERWENT
AN 1991-281056 [38] WPIX
CR 1996-341515 [34]
DNN N1991-214852 DNC C1991-121787
TI **Ferroelectric capacitor** for memory cell - includes diffusion barrier layer to prevent substrate contamination by ferroelectric layer.
DC L03 U14
IN EVANS, J T; KINNEY, W I; MILLER, W D; SHEPHERD, W H
PA (NASC) NAT SEMICONDUCTOR CORP
CYC 1

PI US 5046043 A 19910903 (199138)*
ADT US 5046043 A US 1987-105578 19871008
PRAI US 1987-105578 19871008
AB US 5046043 A UPAB: 19960905
Capacitor for integration with a MOS device comprises a dielectric layer formed on a substrate followed by a diffusion barrier layer, isolation layer, bottom **electrode**, ferroelectric layer and top **electrode**, the barrier layer preventing contamination of the substrate by the ferroelectric layer.

The barrier layer is pref. Si3N4.

The ferroelectric layer is pref. formed on the bottom **electrode** and over an edge so as to be in contact with the isolation layer. The bottom **electrode** has a **Ti**-Pt structure; the isolation layer is TiO2; and the ferroelectric layer is PLZT. Interconnects, pref. having a **TiN-Al** structure, connect the **electrodes** to a MOS device. The capacitor may be offset from the MOSFET or formed above it (not claimed).

USE/ADVANTAGE - In mfr. of a reliable, high density, economical monolithic ferro-electric memory circuit. @(9pp Dwg.No.1/6)@
1/6

L46 ANSWER 6 OF 6 JAPIO COPYRIGHT 2002 JPO
AN 1993-090606 JAPIO
TI SEMICONDUCTOR DEVICE
IN TAKENAKA KAZUHIRO
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 05090606 A 19930409 Heisei
AI JP1991-245859 (JP03245859 Heisei) 19910925
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1412, Vol. 17, No. 434, P. 13 (19930811)
AB PURPOSE: To treat at a high temperature after **Al** of a wiring **electrode** is formed by forming an upper **electrode** of a capacitor made of a ferroelectric material of a conductive film containing Pt as a main ingredient and a laminated structure of **Ti**, **TiN**, etc.
CONSTITUTION: An upper Pt **electrode** 110 is formed in contact with a ferroelectric film 109 by a sputtering method of Pt. An upper **Ti electrode** 111 is formed of **Ti**, TiH by a sputtering method. After an interlayer insulating film between a wiring **electrode** 112 and a **ferroelectric capacitor** is formed, an **Al** wiring **electrode** 113 is formed by a sputtering method. Since the **electrode** 113 is brought into contact with **Ti**, **TiN**, a heat treatment of about 500.degree.C can be performed even after the **Al** **electrode** is formed to be sufficiently durable against formation of a passivation. The Pt is brought into direct contact with the ferroelectric film to improve characteristics of the capacitor. Such a structure is formed thereby to selectively set the **electrode** 110 without considering reactivity with the **Al** of the wiring **electrode**.

L49 ANSWER 1 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 2000-488997 [43] WPIX
DNN N2002-062026 DNC C2002-025405
TI Fabrication of **ferroelectric capacitor** involves forming ferroelectric layer on lower **electrode**, and forming diffusion barrier layer to enclose portions of ferroelectric layer.
DC L03 U11 U12
IN HONG, G; HONG, K
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HONG-I) HONG K
CYC 2
PI KR 99055190 A 19990715 (200043)*
US 2001029101 A1 20011011 (200212)B 5p
ADT KR 99055190 A KR 1997-75102 19971227; US 2001029101 A1 US 1998-221621 19981228
PRAI KR 1997-75102 19971227

AB KR 99055190 A UPAB: 20020226
NOVELTY - Fabrication of **ferroelectric capacitor** involves forming a ferroelectric layer on a lower **electrode**. A diffusion barrier layer is then formed which encloses the rest portions of the ferroelectric layer except for the portion through which the ferroelectric layer will be connected to an upper **electrode**.
DETAILED DESCRIPTION - Fabrication of a **ferroelectric capacitor** involves selectively etching an insulating layer (11) formed on a semiconductor substrate (10) to expose the substrate, and thus form a contact hole. A conductive material (12) is buried in the contact hole to form a first conductive layer. A first diffusion barrier layer is then formed on the entire substrate. A second conductive layer, which is utilized to form a lower **electrode** (17), is also formed over the entire substrate. A ferroelectric layer (18) is formed on the second conductive layer. The ferroelectric layer, the second conductive layer, and the diffusion barrier layer are then patterned. A second diffusion barrier layer (19) is formed on the entire substrate to enclose the ferroelectric layer. Selective etching is then performed on the second diffusion barrier layer to expose the ferroelectric layer at the portion which will be contacted with an upper **electrode**. The upper **electrode** (20) is then formed to connect the ferroelectric layer.

L49 ANSWER 2 OF 2 JAPIO COPYRIGHT 2002 JPO
AN 2000-307072 JAPIO
TI FERROELECTRIC DEVICE
IN IWAMATSU SEIICHI
PA SEIKO EPSON CORP
PI JP 2000307072 A 20001102 Heisei
AI JP1990-127806 (JP2000127806 Heisei) 19900118
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To achieve a ferroelectric device which is free from degradation by forming an insulation film for separating a transistor and a **ferroelectric capacitor** between them and at the same time providing the **ferroelectric capacitor** at the upper layer of the insulation layer and at the upper portion of a position where the transistor is arranged.
SOLUTION: PolySi, **Ti**, W, **TiN**, and the like other than Pt are formed as a lower **electrode** 8 on a C-MOS semiconductor substrate 1 by the sputter method, then an SiN4 film 9 is formed on the lower **electrode** 8 by the plasma **CVD** method, and a

ferroelectric capacitor 10 such as PZT, BaTiO3, Pb5Ge3O11, and Bi4Ti3O12 is formed as a film by the sputtering method. Further, after an Si3N4 11 is formed, an upper **electrode** 12 formed by the same method and material as those of the lower **electrode** 11, and a metal **electrode** such as Al14 is connected to the lower **electrode** 8 and the upper **electrode** 12 for forming via glass 13.

L51 ANSWER 1 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-256436 [30] WPIX
DNN N2002-198431 DNC C2002-076359
TI Plasma etching lead zirconium titanate or barium strontium titanate used in e.g. sensors, involves patterning high-temperature-compatible masking material, and plasma etching using boron chloride and/or tetrachlorosilane.
DC L03 U11
IN HWANG, J H; KAWASE, Y; PARK, S; YAMAUCHI, H; YING, C
PA (MATE-N) APPLIED MATERIALS INC
CYC 21
PI WO 2001082344 A2 20011101 (200230)* EN 23p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
ADT WO 2001082344 A2 WO 2001-US12905 20010420
PRAI US 2000-556078 20000421
AB WO 200182344 A UPAB: 20020513
NOVELTY - Lead zirconium titanate (PZT) or barium strontium titanate (BST) is plasma etched by patterning a layer of high-temperature-compatible masking material overlying the PZT or BST layer; and transferring a pattern from the masking layer through at least a portion of the PZT or BST layer by plasma etching using boron chloride and/or tetrachlorosilane as principal chemical etchant source.

DETAILED DESCRIPTION - Plasma etching PZT or BST layers involves:

(a) patterning a layer of high-temperature-compatible masking material (206) overlying the PZT (204) or BST layer; and

(b) transferring a pattern from the patterned masking layer through at least a portion of the PZT layer by plasma etching the PZT or BST layer through the patterned masking layer using a plasma generated from a plasma feed gas. The principal chemical etchant source is boron chloride (BCl3) and/or tetrachlorosilane (SiCl4).

An INDEPENDENT CLAIM is also included for a plasma etched semiconductor structure including a **ferroelectric capacitor** comprising an upper **electrode** layer, a PZT dielectric layer, and a lower **electrode** layer, having a feature size of less than 0.25 microns m and a sidewall angle of 85-90 deg. .

USE - For plasma etching PZT or BST films used to form dynamic and non-volatile random access memory devices for computers, infrared sensors, and electro-optical devices, particularly **ferroelectric capacitors**.

ADVANTAGE - The masking material can easily be removed without damaging underlying oxides. The selectivity of PZT relative to the masking material (**TiN**) is very good, using BCl3 or SiCl4 with an etch rate ratio of PZT film to **TiN** mask of better than 20:1. The etch rate for PZT using a BCl-3-comprising plasma source gas is in excess of 2000 Angstrom per minute.

DESCRIPTION OF DRAWING(S) - The figure shows a center wafer area of the etched substrate after etching.

Lead zirconium titanate layer 204

Masking material 206

Dwg.2a/3

L51 ANSWER 2 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-178871 [23] WPIX
CR 2002-065449 [72]
DNN N2002-136025 DNC C2002-055372
TI Multilayer **electrode** for **ferroelectric**

capacitor of memory cell e.g. DRAM, has platinum-rhodium layer covered by platinum layer, on substrate.

DC L03 U11 U12
IN AGARWAL, V K; DERDERIAN, G J; GEALY, F D
PA (AGAR-I) AGARWAL V K; (DERD-I) DERDERIAN G J; (GEAL-I) GEALY F D
CYC 1
PI US 2001052608 A1 20011220 (200223)* 21p
ADT US 2001052608 A1 Div ex US 1999-310408 19990512, US 2001-930958 20010817
FDT US 2001052608 A1 Div ex US 6297527
PRAI US 1999-310408 19990512; US 2001-930958 20010817
AB US2001052608 A UPAB: 20020429

NOVELTY - The multilayer **electrode** consists of a platinum-rhodium layer (76) having 3-40% of rhodium and 60-97% of platinum, and covered by a platinum layer (74), on a substrate (50).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Ferro-electric or high dielectric constant capacitor;
(b) Memory cell;
(c) Integrated circuit;
(d) Capacitor lower **electrode** forming method;
(e) Capacitor forming method;
(f) Computer system

USE - Multilayer **electrode** of ferroelectric or high dielectric constant (HDC) capacitor used in memory cell (claimed) e.g. DRAM or FRAM cell of a computer system (claimed) and also in integrated circuit.

ADVANTAGE - By using the platinum-rhodium layer, separation of the **electrode** from the substrate is prevented thereby improving the performance of the capacitor.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **ferroelectric capacitor**.

Substrate 50
Platinum layer 74
Platinum-rhodium layer 76

Dwg.2/22

L51 ANSWER 3 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2002-065449 [09] WPIX
CR 2002-178871 [06]; 2002-215659 [06]
DNN N2002-048604 DNC C2002-019273
TI Ferroelectric or high dielectric constant capacitor for random access memory or ferroelectric random access memory cell, includes platinum-rhodium layer and platinum material layer.
DC L03 U11 U12
IN AGARWAL, V K; DERDERIAN, G J; GEALY, F D
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6297527 B1 20011002 (200209)* 18p
ADT US 6297527 B1 US 1999-310408 19990512
PRAI US 1999-310408 19990512
AB US 6297527 B UPAB: 20020429

NOVELTY - A ferroelectric or high dielectric constant capacitor comprises an **electrode** having a platinum-rhodium layer (76) and a layer consisting of platinum material (74) on top of the platinum-rhodium layer.

USE - For use in a random access memory (RAM) or ferroelectric RAM memory cell and in any integrated circuit requiring capacitors.

ADVANTAGE - The invention possesses a dielectric constant greater (more than 10x) than the conventional dielectrics. It has an advantage of

platinum **electrode** while avoiding problems of oxidation and separation from the substrate. The platinum and platinum-rhodium layers serve as oxidation barriers and exhibits improved adhesion to the substrate, thus providing improved stability and performance of the capacitor.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the **ferroelectric capacitor**.

Upper **electrode** 70
Dielectric layer 72
Platinum material 74
Platinum-rhodium layer 76
Titanium layer 78
Titanium nitride layer 80

Dwg.3/22

L51 ANSWER 4 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2001-305195 [32] WPIX
DNN N2001-219211
TI Method for manufacturing FRAM device - NoAbstract.
DC U11 U14
IN KWON, S Y; YEOM, S J; KWEON, S; YEOM, S
PA (HYUN-N) HYUNDAI ELECTRONICS IND CO LTD
CYC 2
PI KR 2000044671 A 20000715 (200132)*
US 6210979 B1 20010403 (200132)B 11p
ADT KR 2000044671 A KR 1998-61170 19981230; US 6210979 B1 US 1999-474968 19991229
PRAI KR 1998-61170 19981230

AB KR2000044671 A UPAB: 20010615
NOVELTY - A method of fabricating a FRAM device comprises:

(1) forming a first interlayer insulating layer on a semiconductor device having a transistor;

(2) forming a first conductive layer, a ferroelectric layer and a second conductive layer on the first interlayer insulating layer;

(3) forming a **titanium nitride** layer on the second conducting layer and forming a **titanium nitride** pattern layer by selectively etching the **titanium nitride** layer;

(4) forming an upper **electrode** by selectively etching the second conducting layer, where the second conducting layer is etched using the **titanium nitride** pattern layer as etching mask;

(5) forming a capping oxide layer on the **titanium nitride** layer.

USE - Fabrication method for **ferroelectric capacitor**.

ADVANTAGE - Improved adhesive strength between upper **electrode** and capping layer without polymer in FRAM device.

DESCRIPTION OF DRAWING(S) - Drawing shows FRAM device.

silicon substrate 10
oxide layers 11
gate oxide insulating layer 12
gate **electrode** 13
active region 14
bit line 15
first interlayer insulation layer 16
medium temperature insulation layer 17
titanium pattern 18A

first platinum pattern 19A
ferroelectric pattern 20A
platinum upper **electrode** 21A
titanium nitride pattern 22A
capping oxide layer 23
second interlayer oxide layer 24
metal wire 26A
third interlayer insulation layer 27
Dwg.2/2

L51 ANSWER 5 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 2000-022291 [02] WPIX
DNN N2000-016522
TI Iridium oxide local interconnect formation method for a ferroelectric memory cell.
DC U11 U14
IN BAILEY, R A
PA (RAMT-N) RAMTRON INT CORP
CYC 1
PI US 5985713 A 19991116 (200002)* 8p
ADT US 5985713 A Div ex US 1996-618884 19960320, US 1998-183545 19981029
FDT US 5985713 A Div ex US 5838605
PRAI US 1996-618884 19960320; US 1998-183545 19981029
AB US 5985713 A UPAB: 20000112
NOVELTY - Conductive layers are formed extending adjacent from the source or drain contacts of a transistor but not making contact with the **electrode** contact of a **ferroelectric capacitor** . An iridium oxide local interconnect is formed over the conducting layer.
DETAILED DESCRIPTION - The iridium oxide local interconnect extends from the source or drain contacts of the transistor to the **electrode** contact of the **ferroelectric capacitor** . The ends of the conductive layers are laterally terminated not less than one-half micron from the **electrode** contact. The conductive layer comprises an iridium layer formed over a **titanium nitride** layer.
USE - For forming iridium oxide local interconnect for a ferroelectric memory cell.
ADVANTAGE - Minimizes ferroelectric degradation due to dissociation of water molecules to form hydrogen. Maintains low resistivity since the conductive layer extends below the local interconnect from the source or drain contact adjacent to the upper **electrode** contact of the **ferroelectric capacitor**.
DESCRIPTION OF DRAWING(S) - The figure shows a sequential cross-sectional view of the ferroelectric memory cell.
Dwg.10/10

L51 ANSWER 6 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1999-253979 [21] WPIX
CR 1996-362224 [36]; 1997-525797 [48]; 1998-505779 [43]
DNN N1999-189062
TI **Ferroelectric capacitors** for memory system of computer.
DC U12 U13 U14
IN EVANS, J T; WOMACK, R H
PA (RADI-N) RADIANT TECHNOLOGIES
CYC 1
PI US 5892255 A 19990406 (199921)* 8p
ADT US 5892255 A Cont of US 1996-661597 19960611, US 1997-946749 19971012

FDT US 5892255 A Cont of US 5679969
PRAI US 1996-661597 19960611; US 1997-946749 19971012
AB US 5892255 A UPAB: 19990603
NOVELTY - The top and bottom **electrodes** are sandwiched through a dielectric material of Curie point less than 400 deg. C. The dielectric material is surrounded by a barrier to prevent the leaving or entering of oxygen. Drain terminal of FET (104) is connected to bottom **electrode** through **titanium** or **titanium nitride** layer.
USE - The single bit memory cell of computer memory system.
ADVANTAGE - Since dielectric layer is surrounded by oxygen, the shift in hysteresis curve along voltage axis and fatigue is prevented.
DESCRIPTION OF DRAWING(S) - The figure shows memory cell utilizing the **ferroelectric capacitor**.
FET 104
Dwg.1/8

L51 ANSWER 7 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1999-203967 [17] WPIX
DNN N1999-150226 DNC C1999-059304
TI IC memory device manufacture useful for DRAM's and FRAM's.
DC L03 U11 U13 U14
IN KIM, B H; LEE, S M; OH, S J; PARK, I S; KIM, B; LEE, S; OH, S; PARK, I
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 3
PI US 5879982 A 19990309 (199917)* 7p
JP 10178157 A 19980630 (199917) 7p
KR 98048379 A 19980915 (199941)
KR 219507 B1 19990901 (200104)
ADT US 5879982 A US 1997-948566 19971010; JP 10178157 A JP 1997-301633 19971104; KR 98048379 A KR 1996-66950 19961217; KR 219507 B1 KR 1996-66950 19961217
PRAI KR 1996-66950 19961217
AB US 5879982 A UPAB: 19991116
NOVELTY - The method involves forming **TiN** diffusion barrier regions (117) in the bottom of vias formed in a second insulating layer that expose regions of a second **electrode** and a first interconnect layer. The exposed parts of the second **electrode** and the first interconnect layer in the vias are then patterned.
DETAILED DESCRIPTION - Forming an IC memory device comprises:
(a) forming a first insulating layer (103) on a semiconductor substrate (101) containing memory cells in an array region, and peripheral circuits for driving the array in a peripheral circuit region;
(b) patterning a first conductive layer (109) to form a first capacitor **electrode** (109a) extending opposite the array and a first interconnect layer (109b) opposite the peripheral region;
(c) forming a dielectric layer (111) on the first **electrode**;
(d) forming a second capacitor **electrode** (113') on the dielectric region opposite the first **electrode**;
(e) forming a second insulating layer (115) on the second **electrode** layer and the first interconnect layer;
(f) forming first and second vias in the second insulating layer to expose the second **electrode** and the first interconnect layer; and
(g) patterning the second conductive layer in the first and second vias.
USE - For DRAM's and FRAM's (ferroelectric random access memory).

ADVANTAGE - The polarization characteristics of the **ferroelectric capacitor** are not degraded by **Ti** diffusion. Using the lower **electrode** as a metal interconnect in the peripheral circuit region eliminates the need for an ohmic layer to couple interconnects, reduces contact resistance in the peripheral circuit region and further reduces degradation of the polarization characteristics of the **ferroelectric capacitor**.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-section of the device formed by the above method.

Semiconductor substrate 101
First insulating layer 103
First conductive layer 109
First capacitor **electrode** 109a
First interconnect layer 109b
Dielectric layer 111
Second capacitor **electrode** 113'
Second insulating layer 115
Diffusion barrier region 117

Dwg.2D/2

L51 ANSWER 8 OF 11 WPIX (C) 2002 THOMSON DERWENT
AN 1995-131516 [17] WPIX
DNN N1995-103323
TI Connecting silicon substrate to electrical component via platinum conductor - bonding barrier layer of **titanium** compound to silicon substrate, layer of platinum bonded to barrier layer comprising single crystal.
DC U11 U13 U14
IN BULLINGTON, J A; EVANS, J T
PA (RADI-N) RADIANT TECHNOLOGIES INC; (RADI-N) RADIANT TECHNOLOGIES
CYC 21
PI WO 9508187 A1 19950323 (199517)* EN 14p
RW: AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
W: AU CA JP KR
AU 9474784 A 19950403 (199529)
US 5440173 A 19950808 (199537) 7p
ADT WO 9508187 A1 WO 1994-US8681 19940728; AU 9474784 A AU 1994-74784 19940728; US 5440173 A US 1993-123289 19930917
FDT AU 9474784 A Based on WO 9508187
PRAI US 1993-123289 19930917
AB WO 9508187 A UPAB: 19950508
A cell (30) is constructed by constructing a CMOS transistor (32) with drain (33), gate region consisting of a gate oxide (35), gate **electrode** (36) and source (34). The gate structure are insulated with a glass layer (37). A capacitor (40) is constructed by depositing a bottom **electrode** (42) on source (34). A ceramic layer (43) is deposited and sintered then a top **electrode** (41) deposited.

The structure is heated in the presence of oxygen to over 800 deg. C without destroying electrical connection. A **Tin** or TiW buffer layer connects a platinum conductor to the silicon substrate.

USE/ADVANTAGE - Semiconductor memories. Improved contact withstanding high temperature in presence of oxygen.

Dwg.2/4

L51 ANSWER 9 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1999-274406 JAPIO
TI METHOD FOR FORMING **FERROELECTRIC CAPACITOR**
IN KAN UN YORU

PA HYUNDAI ELECTRONICS IND CO LTD
PI JP 11274406 A 19991008 Heisei
AI JP1998-377707 (JP10377707 Heisei) 19981229
PRAI KR 1997-77974 19971230
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To prevent a ferroelectric thin film from being broken at a time of forming a **ferroelectric capacitor**, by a method wherein a SBT thin film for preventing impurities diffusing from a SBT ferroelectric thin film formed above a lower **electrode** to the outside is selectively etched, and the SBT ferroelectric thin film is brought into contact with an upper **electrode**.
SOLUTION: After a **Ti** film 28 and a **TiN** film 29 which comes into direct contact with a polysilicon film 27 are formed of a barrier metal film, a first platinum **electrode** 30 and a SBT ferroelectric thin film 31 are laminated in this order, and after a photomask step, the SBT ferroelectric thin film 31, the first platinum **electrode** 30, the **TiN** film 29 and the **Ti** film 28 are etched in this order. Next, a diffusion barrier film is formed above the entire structure with a SBT film 32 by a sputtering method. Next, a TiO<SB>2</SB>, film 33 having more excellent impurity invasion prevention characteristic is formed above the SBT film 32. Finally, thc TiO<SB>2</SB> film 33 and the SBT film 32 are etched in order to expose the ferroelectric thin film 31 and a second platinum **electrode** 34 is formed to complete FeRAMs.

L51 ANSWER 10 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1994-029461 JAPIO
TI CAPACITOR STRUCTURE OF SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN KASHIWABARA KEIICHIROU; TSUCHIMOTO JUNICHI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 06029461 A 19940204 Heisei
AI JP1992-181203 (JP04181203 Heisei) 19920708
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1544, Vol. 18, No. 238, P. 145 (19940506)
AB PURPOSE: To provide an **electrode** structure of a **ferroelectric capacitor** having a structure which has excellent heat resistance.
CONSTITUTION: A pair of silicon layers 1 and 2 are opposed through a ferroelectric element layer 10. A **titanium nitride** layer 9 is so formed as to be interposed between at least one of the layers 1, 2 and the layer 10. The layer 9 is formed of an isometric crystal.

L51 ANSWER 11 OF 11 JAPIO COPYRIGHT 2002 JPO
AN 1992-085878 JAPIO
TI SEMICONDUCTOR DEVICE
IN KATO KOJI
PA SEIKO EPSON CORP, JP (CO 000236)
PI JP 04085878 A 19920318 Heisei
AI JP1990-198797 (JP02198797 Heisei) 19900726
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1229, Vol. 16, No. 3, P. 89 (19920707)
AB PURPOSE: To prevent a drop in reliability accompanying oxidation of an **electrode** base material annealed in an oxygen atmosphere by using an oxide conductor for an **electrode** of a **ferroelectric capacitor**.
CONSTITUTION: When a non-volatile memory which uses a metal

electrode, such as platinum and a barrier metal, such as **titanium** and **titanium nitride**, is annealed in an oxygen atmosphere of 600.degree.C for one hour, peeling occurs at an **electrode** in the lower pat of metal, such as platinum. To comply with this, an oxide conductor, such as ITO (mixture of indium oxide and stannic oxide) is used at least as a lower **electrode** 10, which makes it possible to cut off the diffusion of oxygen. Therefore, the oxidation of a barrier metal 9, such as **titanium** or **titanium nitride** will not take place even after it is annealed.